2.5D and 3D Integration Technology and Applications

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Effective End of Moore's Law

Moore's Law was first and foremost a statement about economics. We could shrink transistors and build more of them for about the same cost.

- This has been the basic premise of the semiconductor industry for 50 years and was true up until the last few years.
- Today we can indeed shrink transistors further, but the cost per transistor no longer declines.

  We can get something a little more compact
  - Perhaps a little less power
  - But we pay more for these features now.

NHANCED SEMICONDUCTORS

What Does This Mean?

The semiconductor industry is about to undergo a sea change.

- New ways of accomplishing Moore’s law economics and performance are needed.
  - The industry is now looking to use advanced packaging to drive future semiconductors.
    - Better Cost
    - Better Performance
    - Better SWaP

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Vision of the Future

A new semiconductor industry paradigm is evolving…

Foundry 2.0 –

A Finishing Foundry that takes the standardized building blocks from traditional semiconductor manufacturers and uses advanced packaging and additive manufacturing to create highly customized components with superior performance targeting small and medium sized markets.

Foundry 1.0 – Todays Model

- Current semiconductor business has been focused on driving smaller transistors.
  - High development cost
  - High capital cost
  - Long development times
  - Expensive design tools
  - High risk
- Twilight of Moore's Law

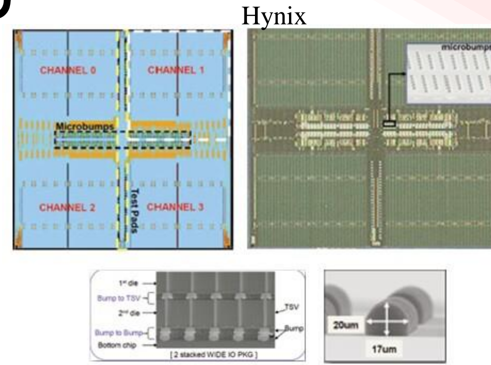
Foundry 2.0 – New Model

- System solution focus
  - Best of class components
  - Additive Semiconductor Processing
- Relies on Advanced Packaging (AP) and Chiplets
  - Heterogenous integration
  - Photonics
  - MEMS
  - RF
- Advantages
  - Low development cost
  - Low capital cost
  - Short development times
  - Inexpensive design tools
  - Low risk

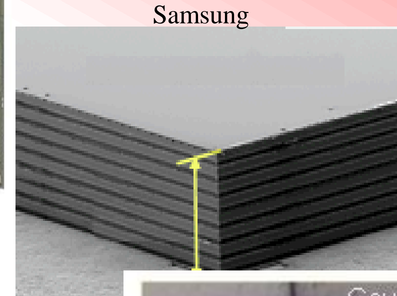
What Is Advanced Packaging?

- Sensors (Cameras)
  - Sony 10+ years ago, - now mainstream
  - Virtually every new USG IR sensor is an AP
  - Driven by size/form factor
  - System cost reduction
- GPUs
  - Dawn of both interposers and chiplets
- Micro-Displays
  - Driven by materials (GaN) and pitch requirements
- Compute Devices
  - leading edge risk takers
  - AMD and Xilinx early and now Intel
  - Driven by
    - Memory BW/Latency
    - Heterogenous targeted compute
    - Photonics coming on scene for I/O and compute
  - Lower power per bit-op
  - Effective Larger die with much better yield/cost

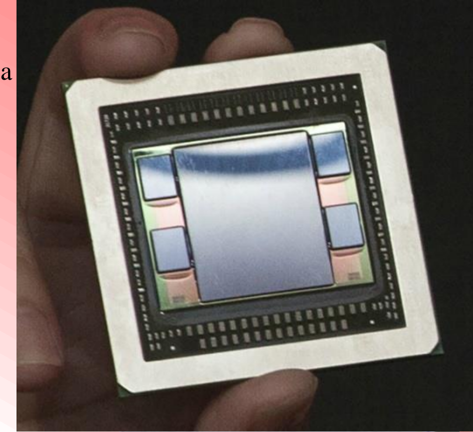
Hynix

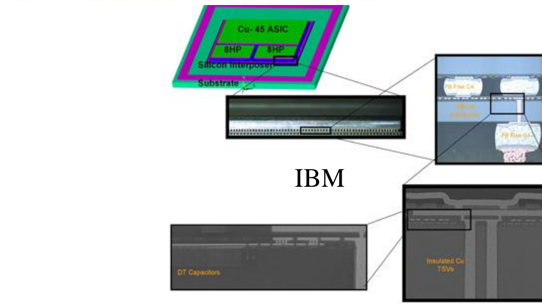


Samsung

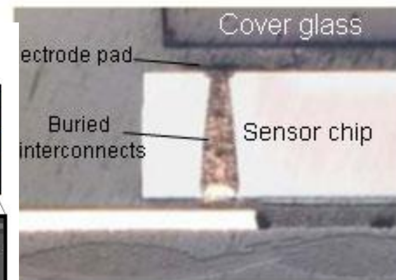


nVidia

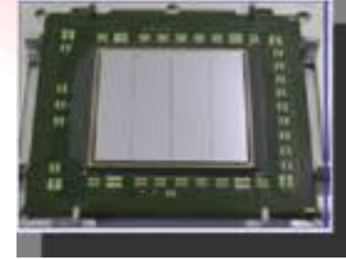




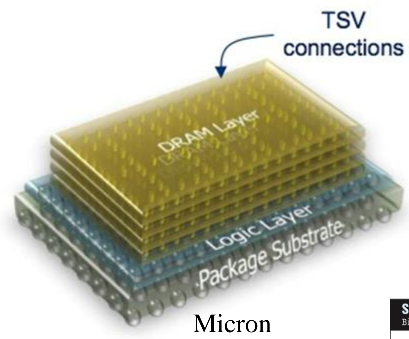
IBM



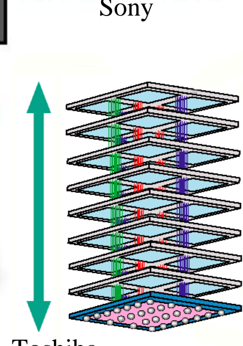
Sony



Xilinx



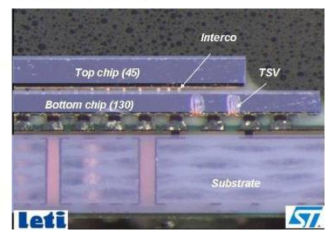
Micron



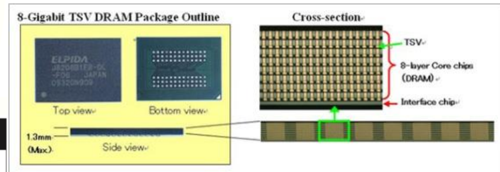
Toshiba

Structure of Toshiba's new NAND memory cell

BiCS tech helps create a SONOS memory structure



STMicro



Elpida

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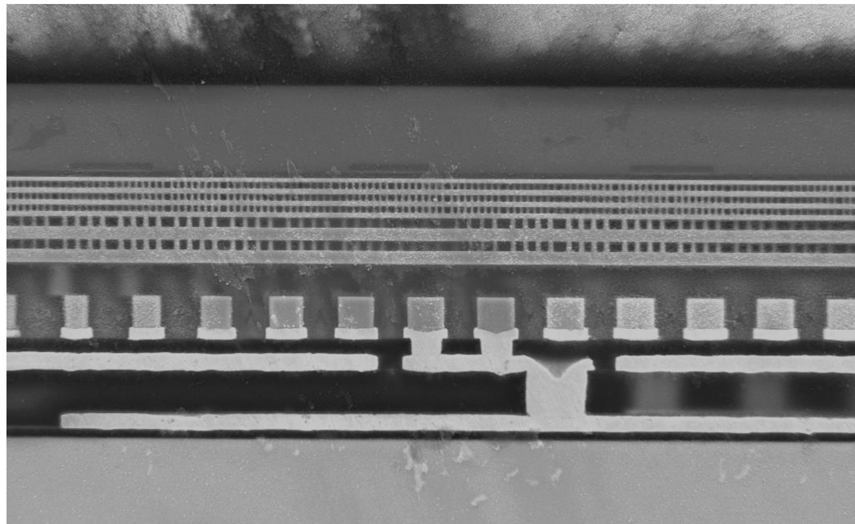
AP Elements: Bonding

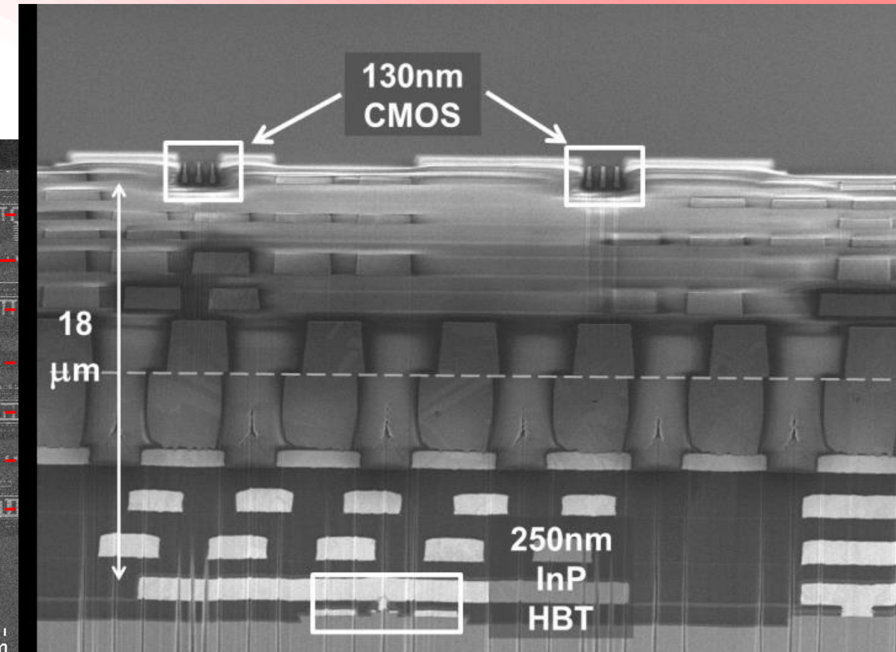
Millimeters ⇨ Microns

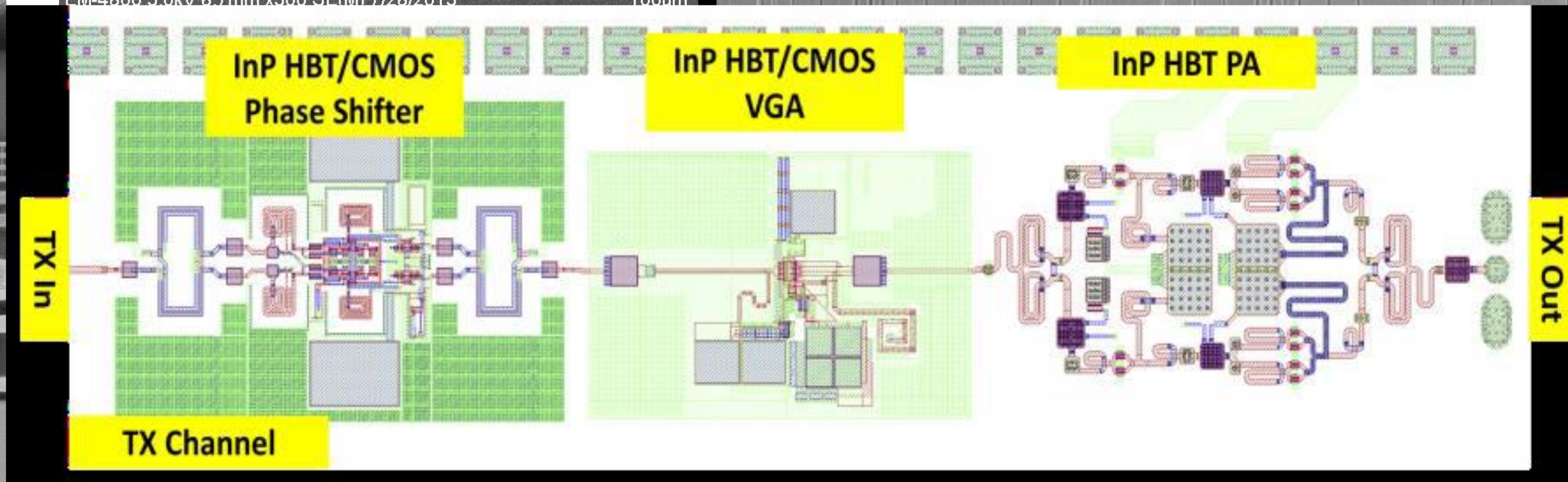
Kilograms ⇨ Grams

Mixed Materials

Best of Class

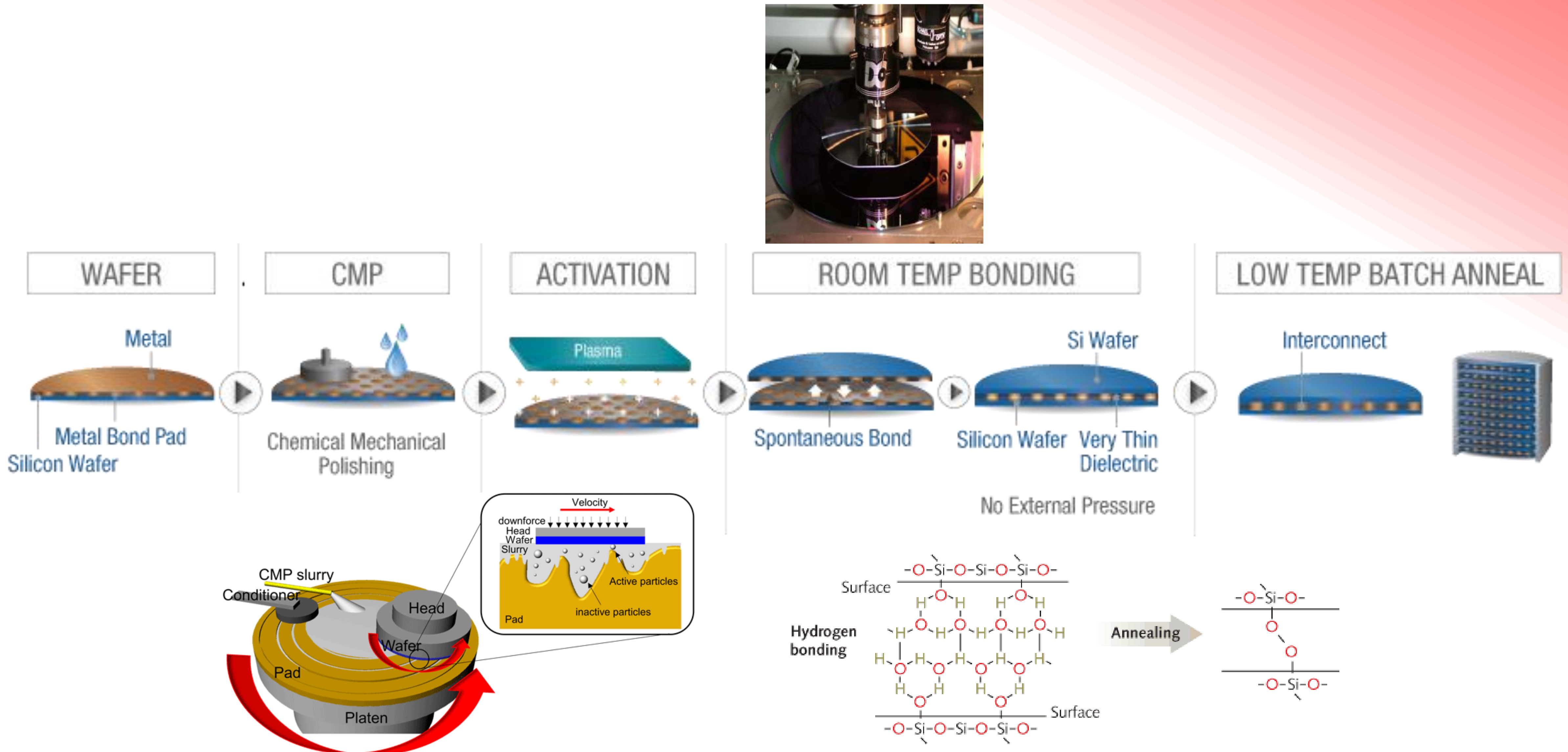






NHANCED SEMICONDUCTORS

DBI®: Low Temperature Hybrid Bonding Process



Jihoon Seo / Materials Research Society

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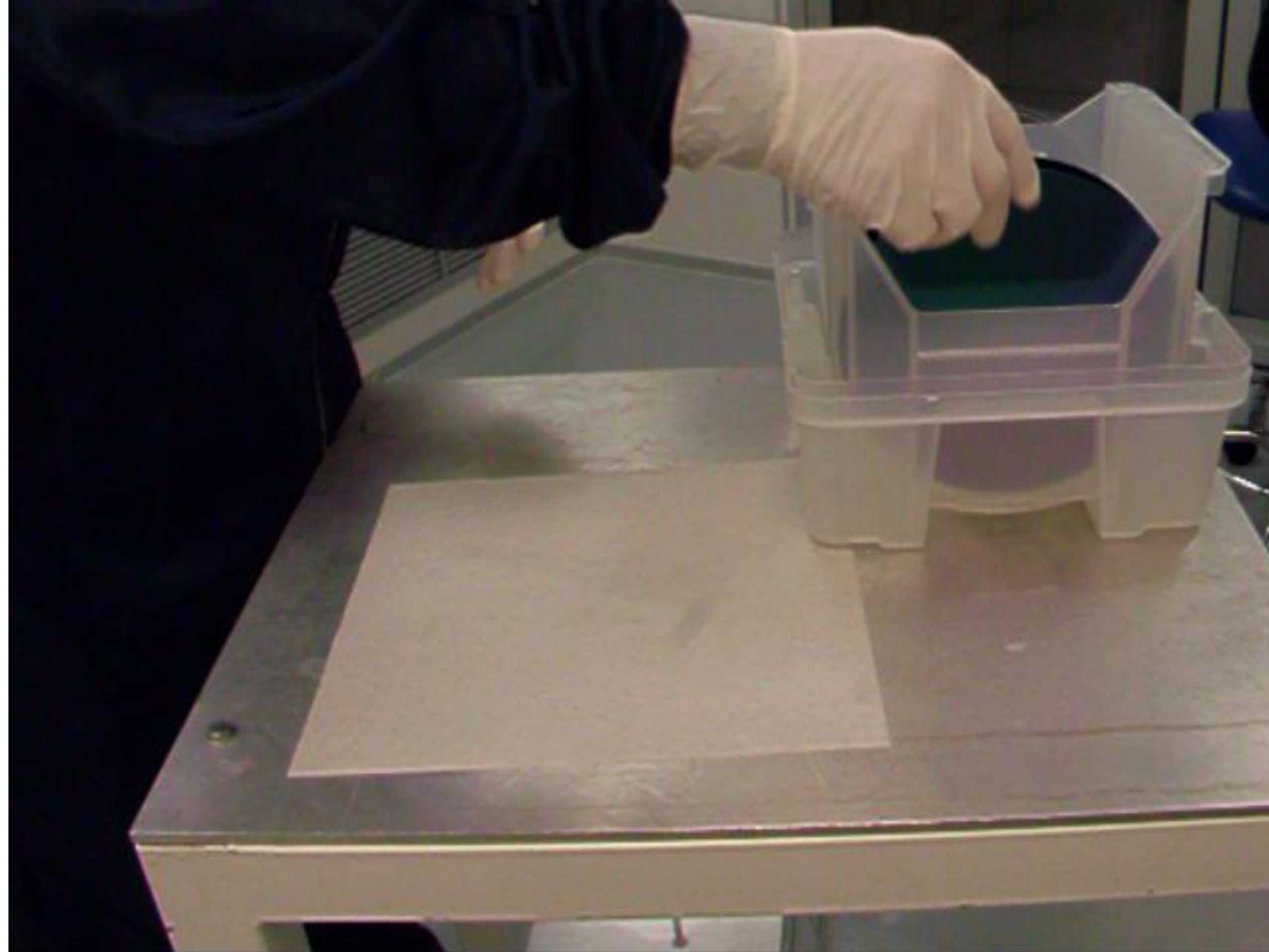
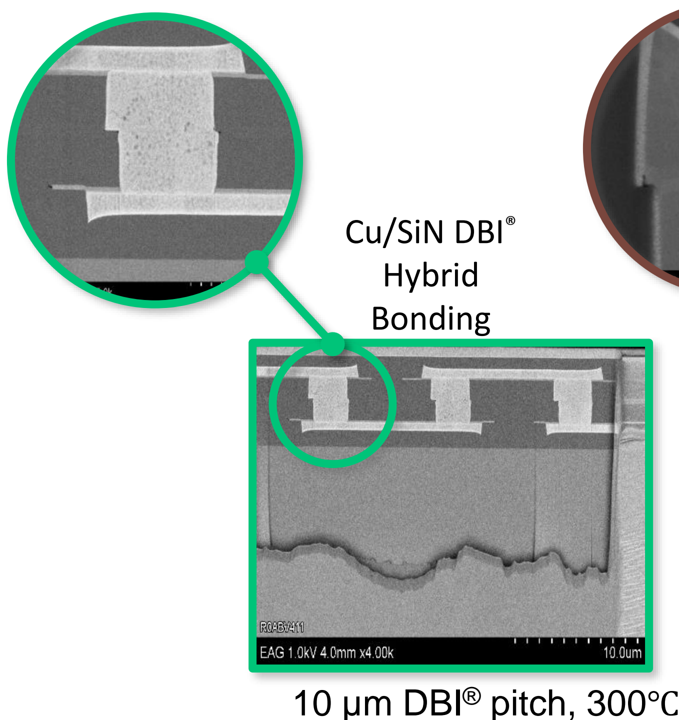
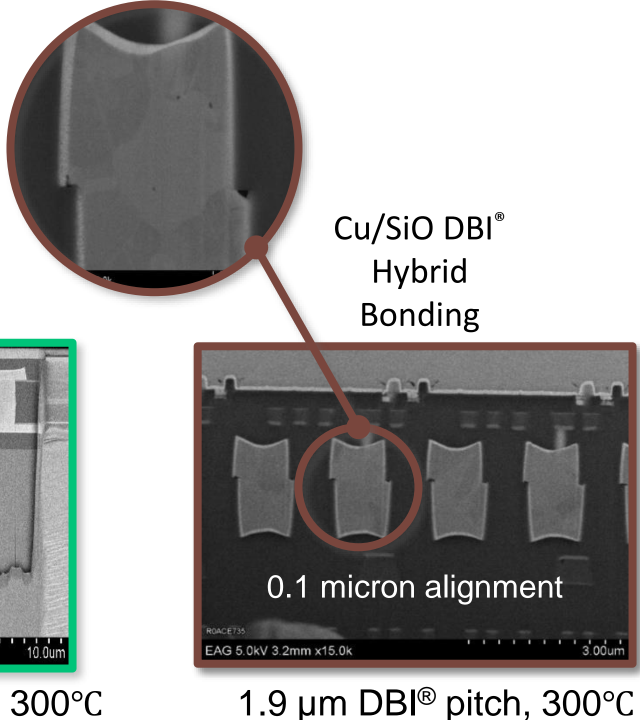
Bonding in Action



Hybrid Bonding Interconnect Pitch Scaling

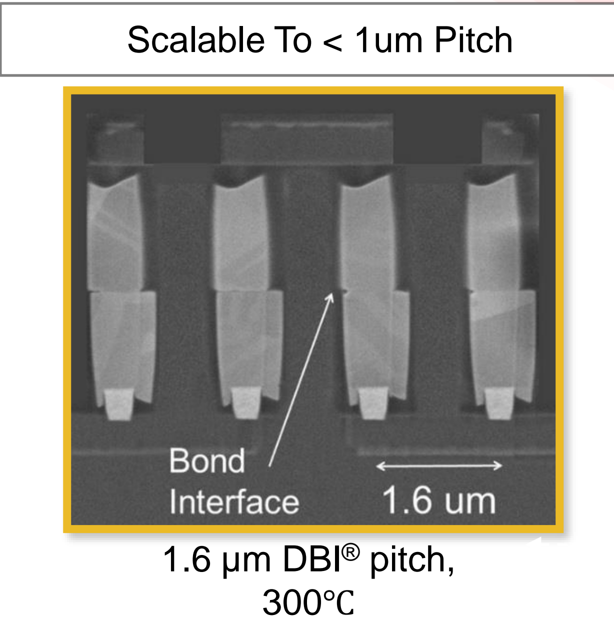


10 μm DBI® pitch, 300℃



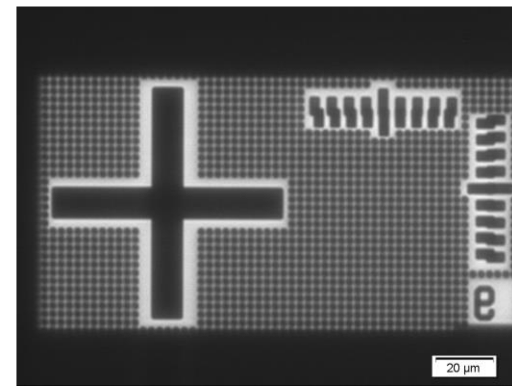
1.9 μm DBI® pitch, 300℃

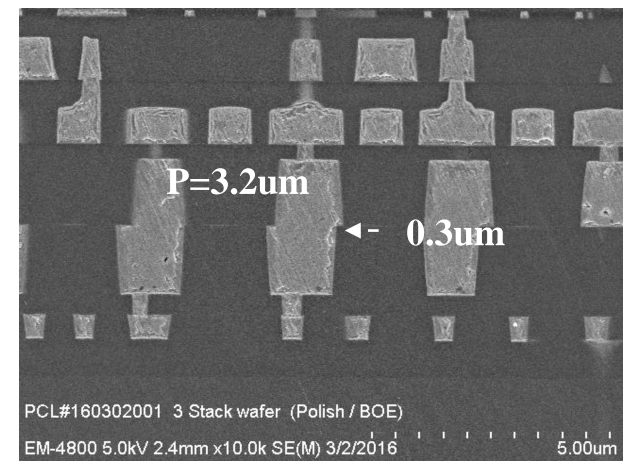
Scalable To < 1um Pitch



1.6 μm DBI® pitch, 300℃

- 3sigma < +/- 1um misalign performance
- Production Minimum pitch = 2.44um
- Best alignment is achieved with face-to-face bonding

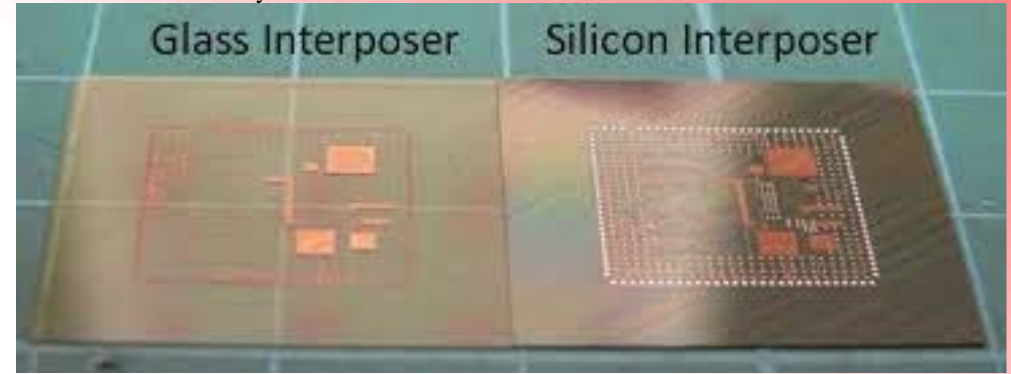


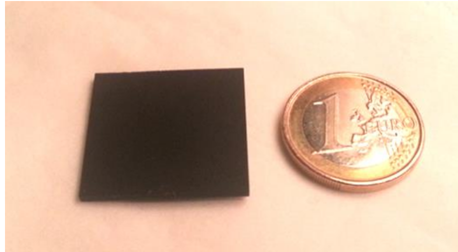


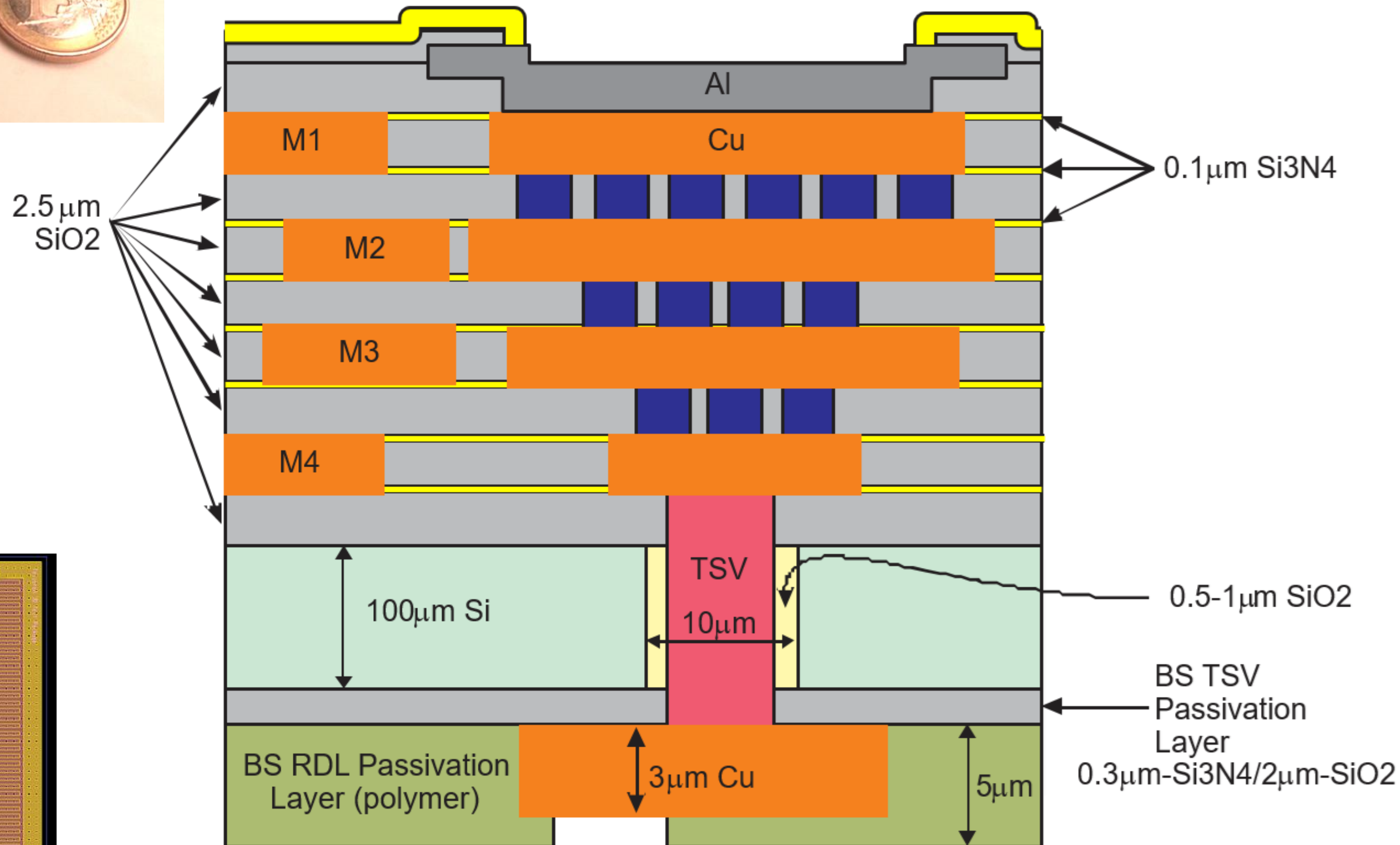
AP Elements: Interposers

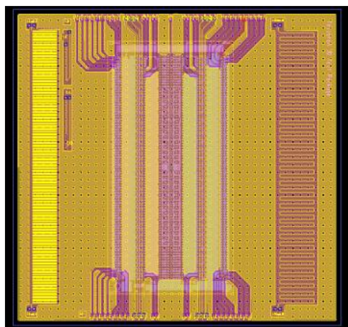
- ➢Bigger, Better, Faster
- ➢Lower Power

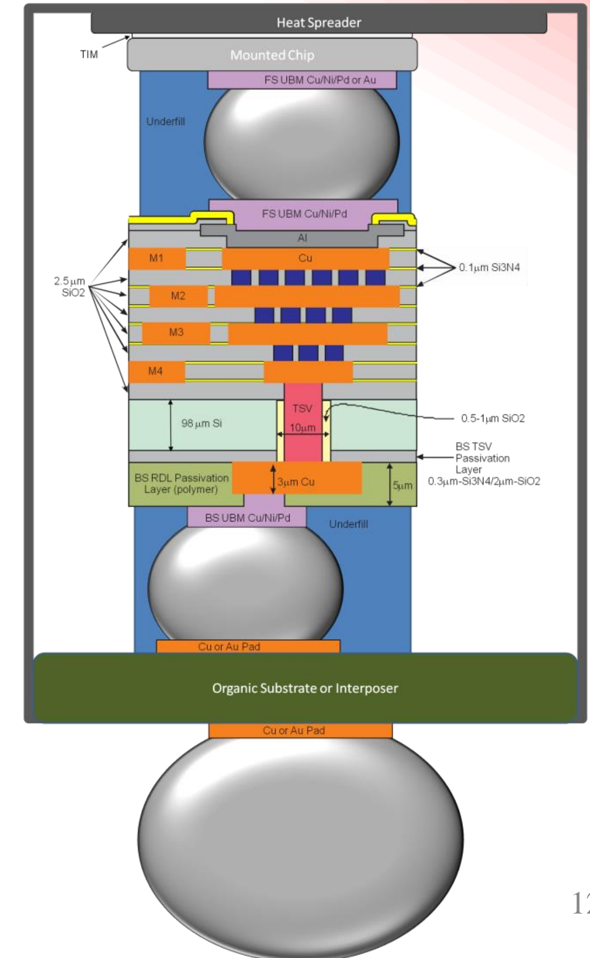
Mosaic Microsystems











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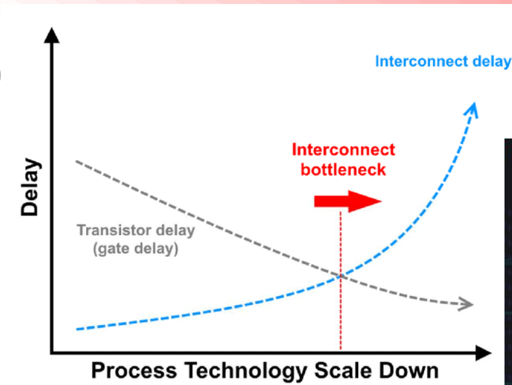
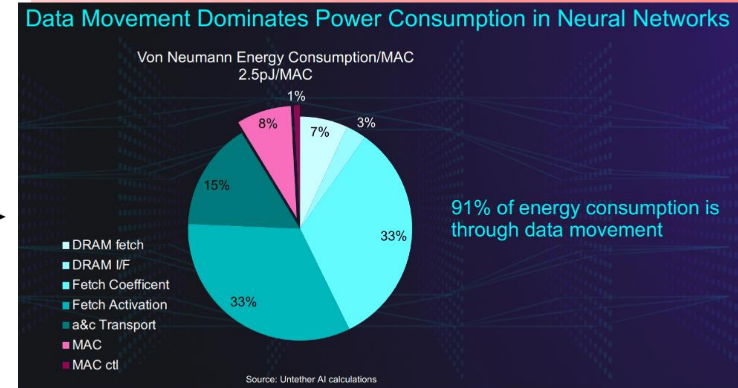
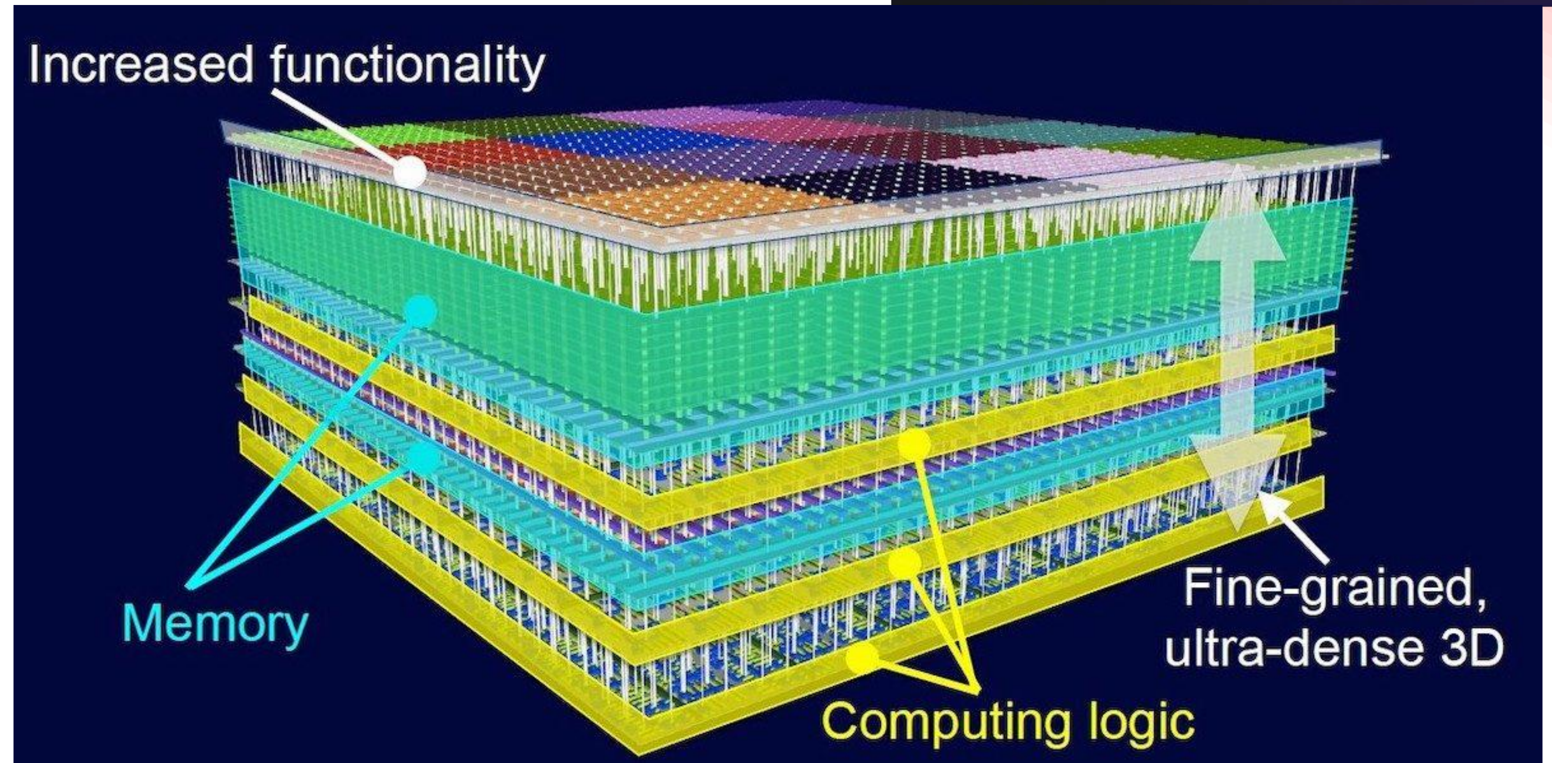
AP Elements: Wiring (Metallization)

- Wire length controls the delay
  - Span of control
- Accounts for majority of power usage
  - Memory fetch

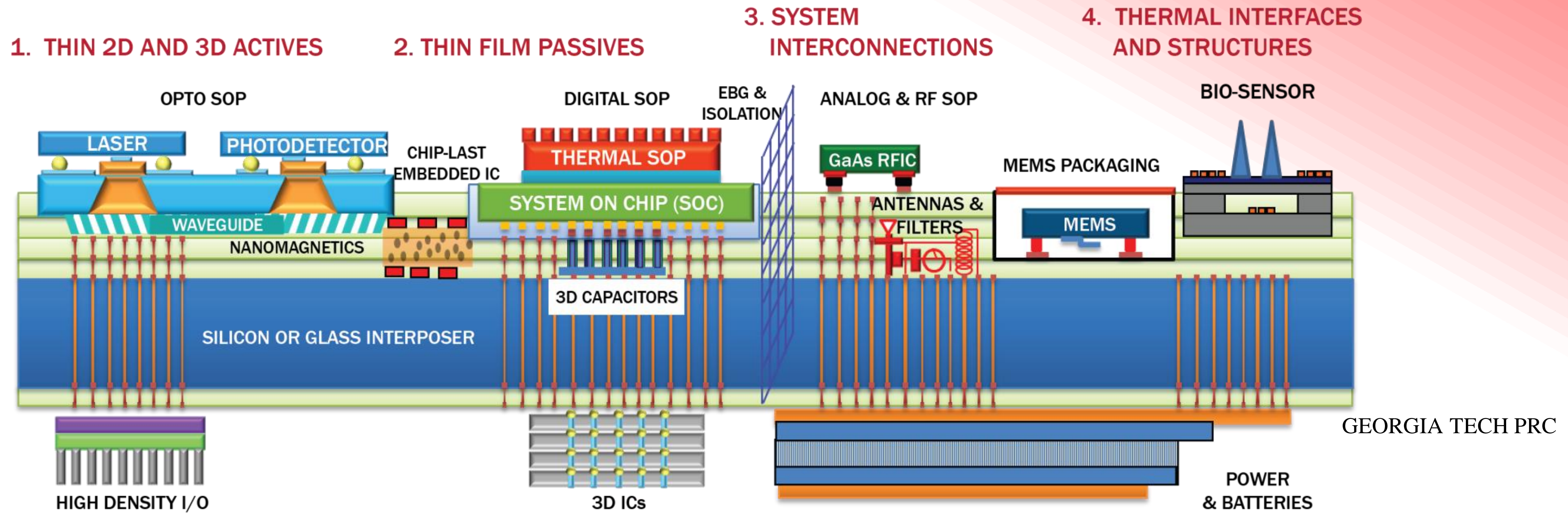


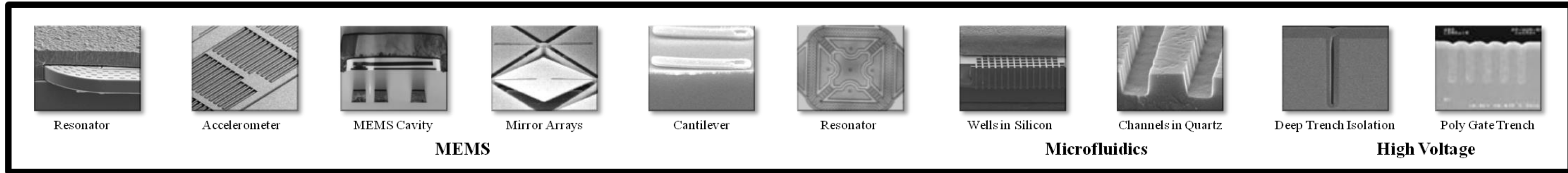


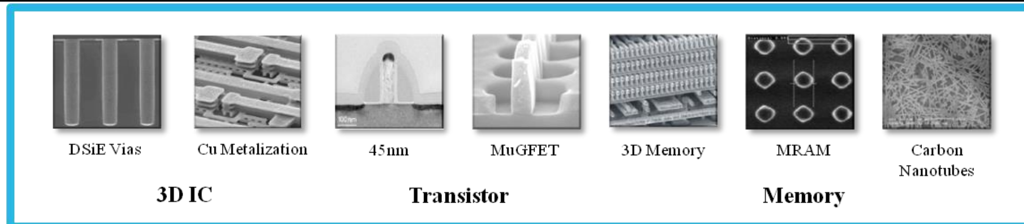


3DInCities

More Than Moore Technologies

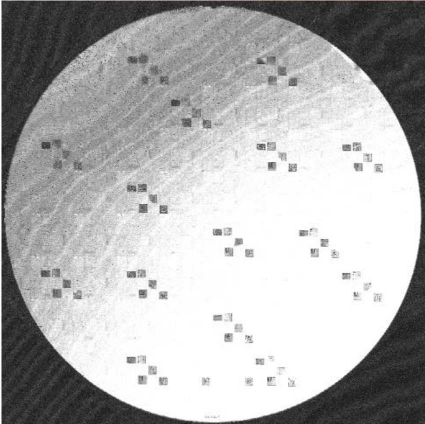


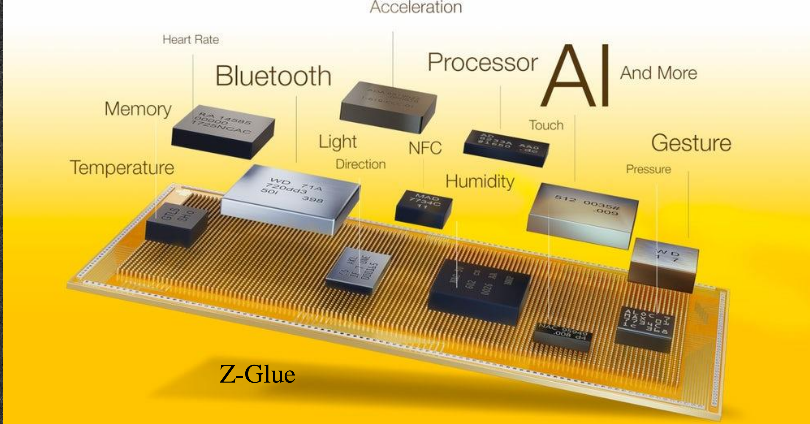




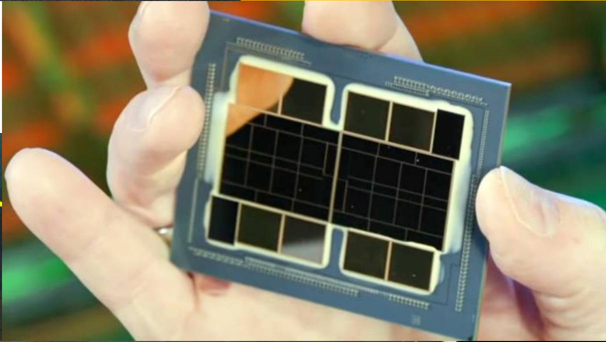
AP Components: Chiplets

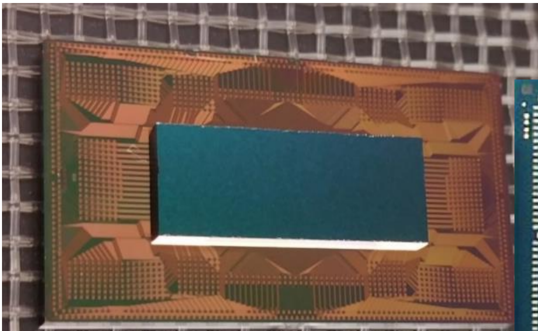
- Best of Class Everything
- Easy retargeting
- Lower risk
- IP reuse
- Lower cost

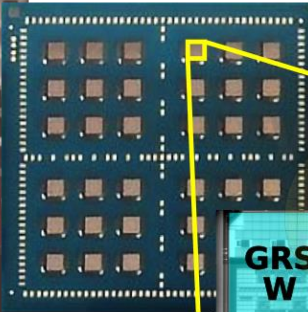


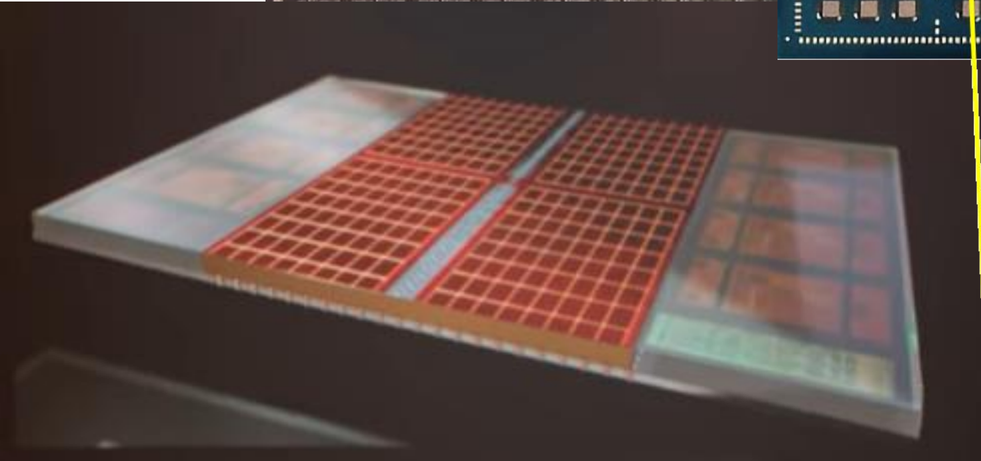


Z-Glue


Intel






AMD

GRS W | GRS N | GPIO | GRS N | GRS E
GB | PE | PE | PE | PE
RISC-V | PE | PE | PE | PE
PE | PE | PE | PE
PE | PE | PE | PE
GRS W | GRS S | JTAG | GRS S | GRS E

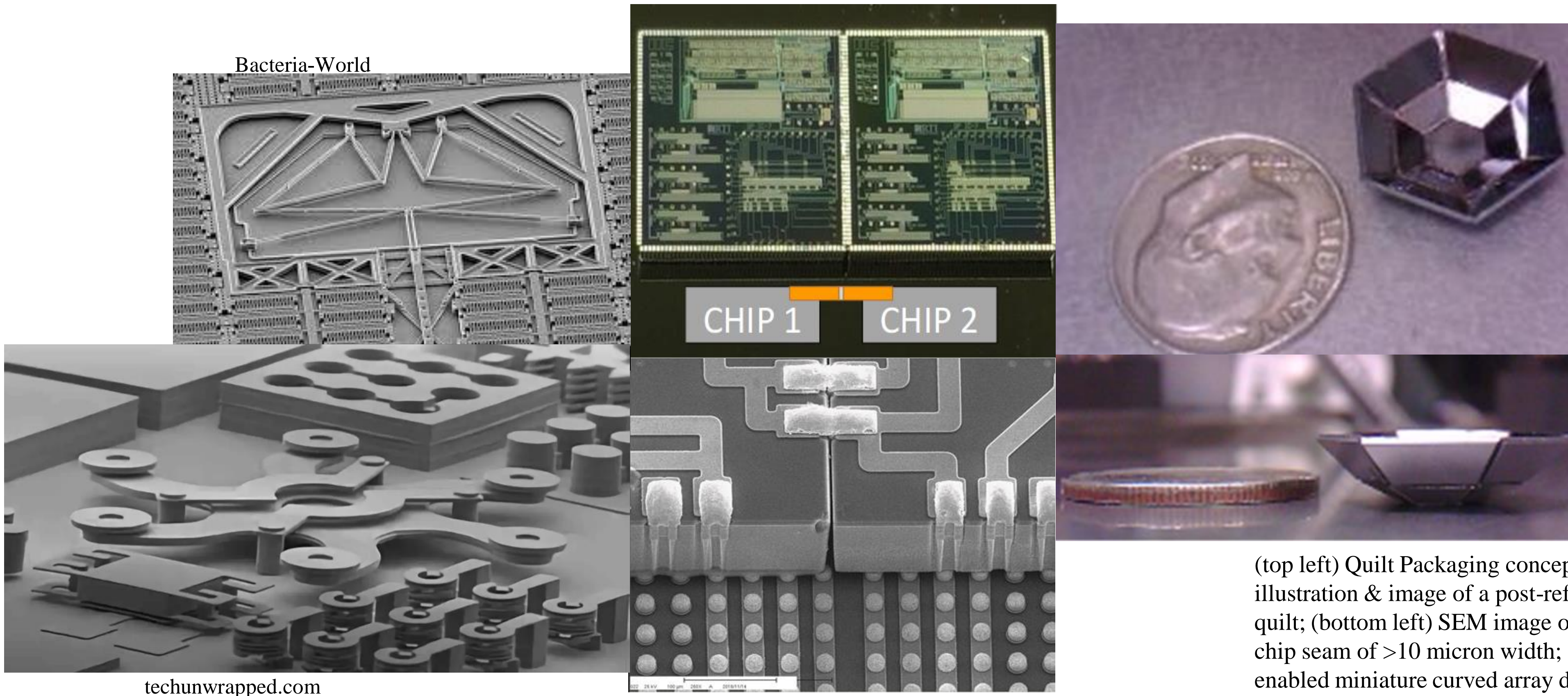
nVidia

Intel

AP Components Micro-Connections and 3D Structures

MEMS + Precision Electronics

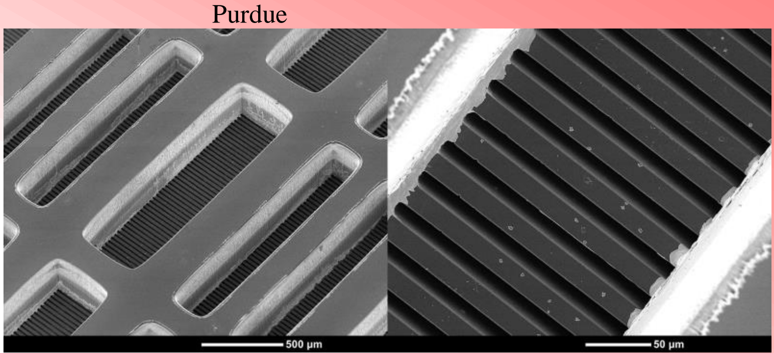
IIC



(top left) Quilt Packaging concept cross-section illustration & image of a post-reflowed QP CMOS quilt; (bottom left) SEM image of quilted chip-to-chip seam of >10 micron width; (top right) QP-enabled miniature curved array demonstration article; (bottom right) profile view of QP-enabled miniature curved array.

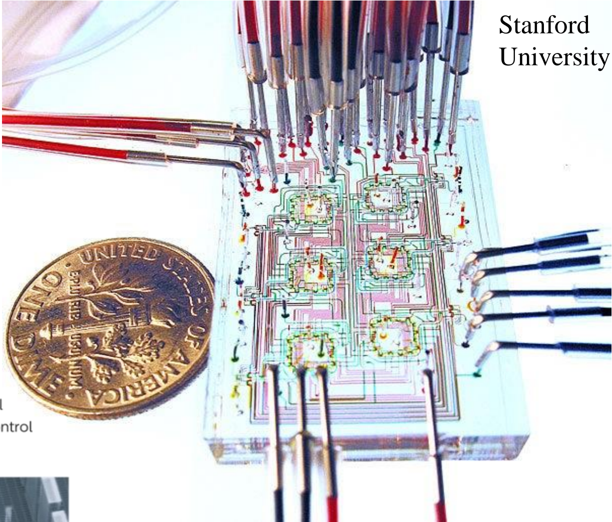
NHANCED SEMICONDUCTORS

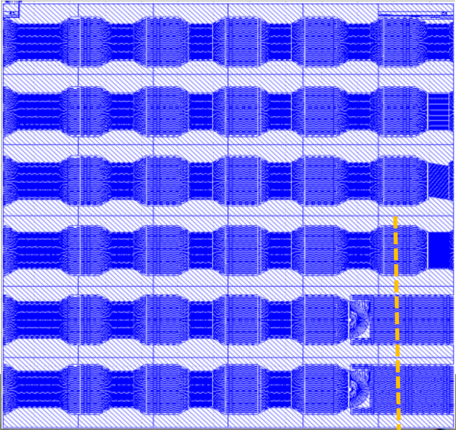
AP Components: Microfluidics and Cooling

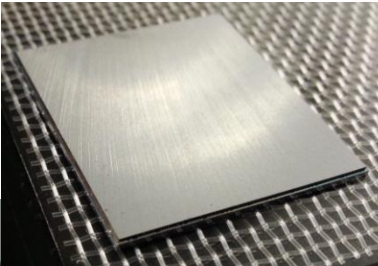


Chip Scale Cooling
For Ultra-Dense Electronics

Biology + Electronics

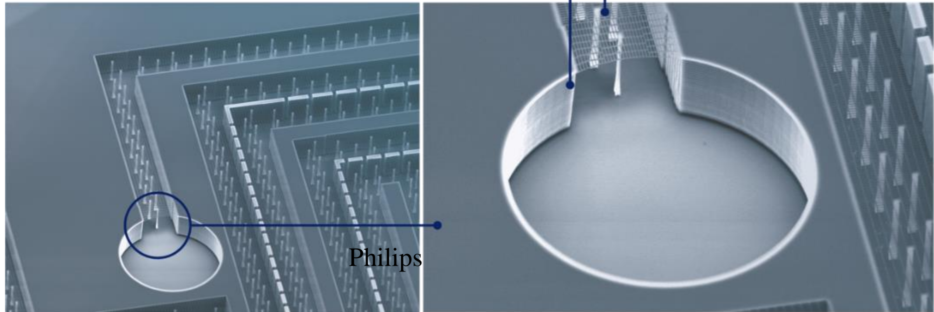






Our state-of-the-art tool set enables us to create microfluidic structures with accurate control:

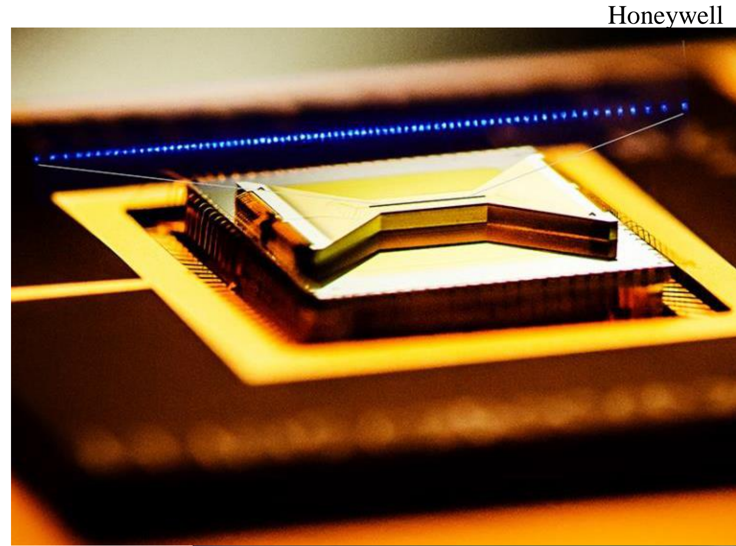
- <5 degree slope control
- Sub-µm feature size control
- µm range feature size



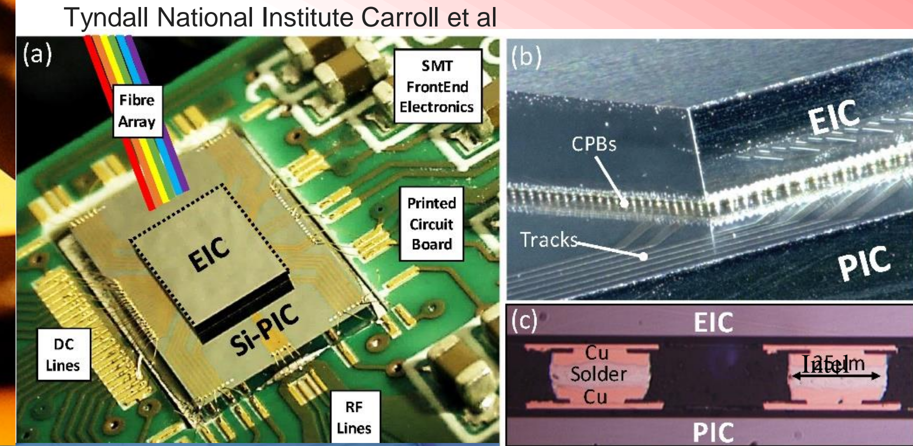
AP Components: Photonics & Quantum

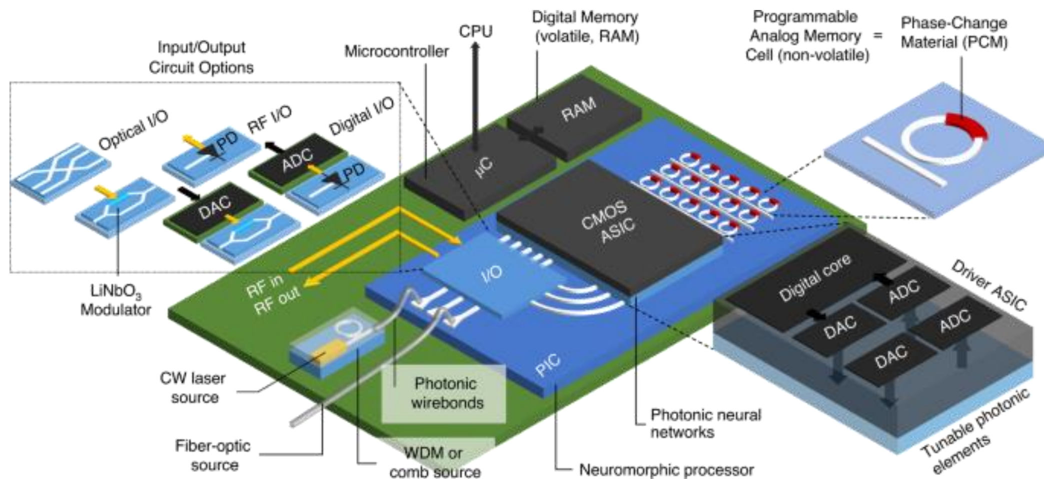
- I/O
  - Tb/s, <<100fJ/b
    - SiP 500ff I/O Load
    - 2.5D 25ff I/O Load
    - 3D 3ff I/O Load
- Processing
  - "Quantum Leaps"

Honeywell

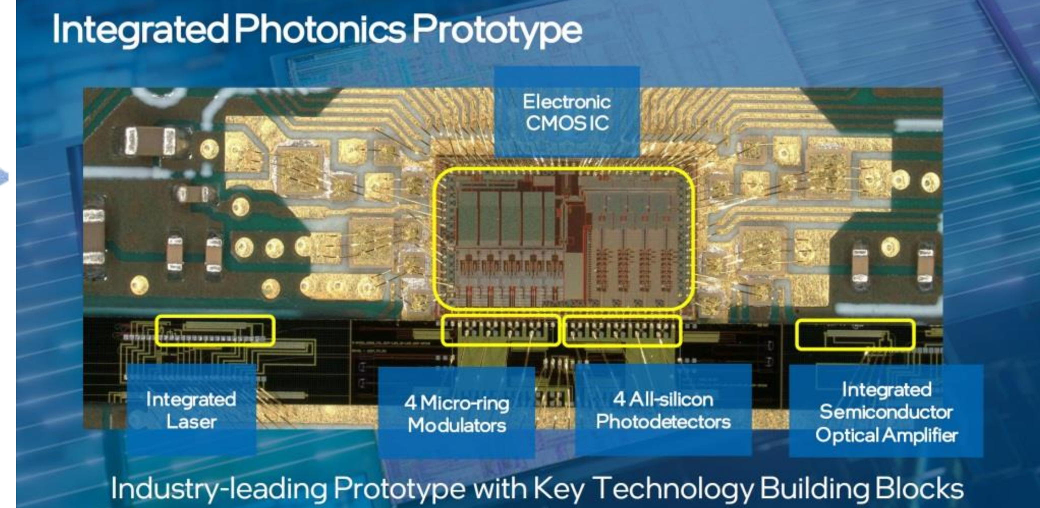


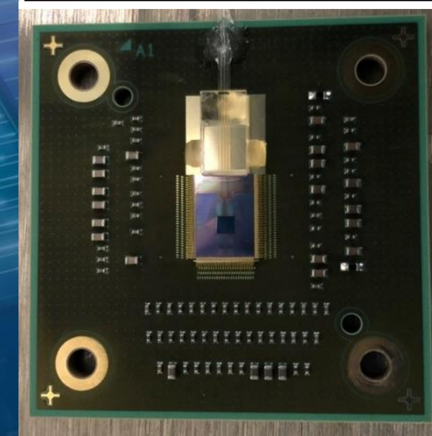
Tyndall National Institute Carroll et al





Nature 29 January 2021 Shastri

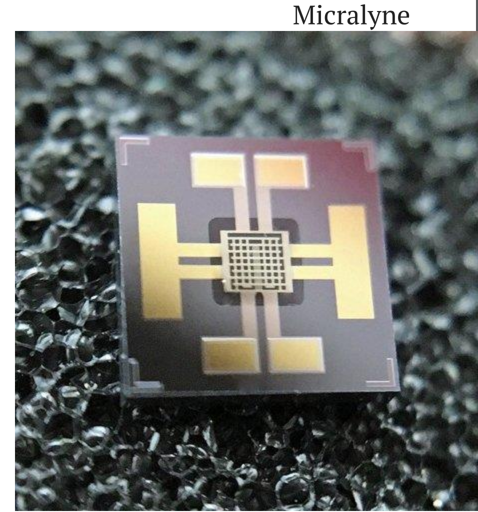




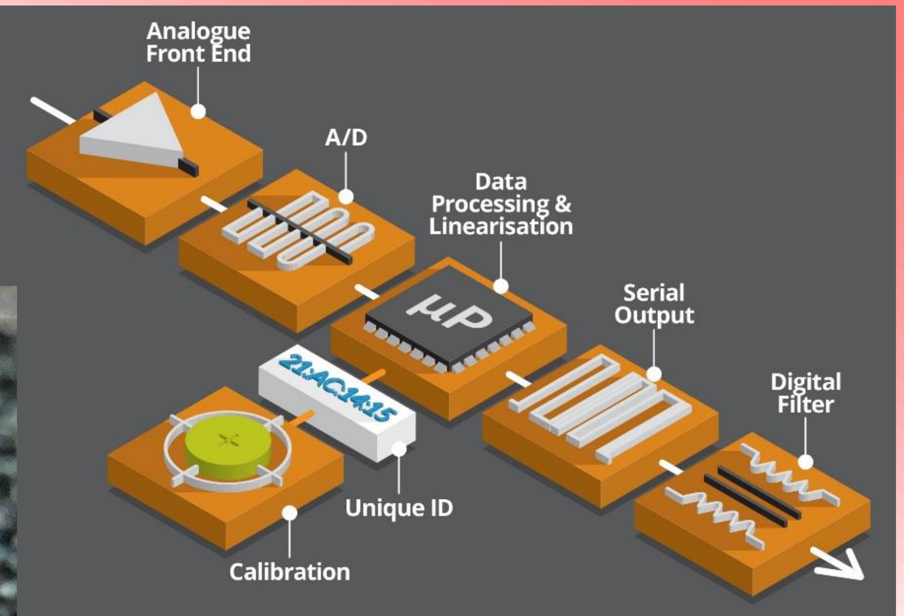
NHANCED SEMICONDUCTORS

Intelligent Sensors and Edge Compute

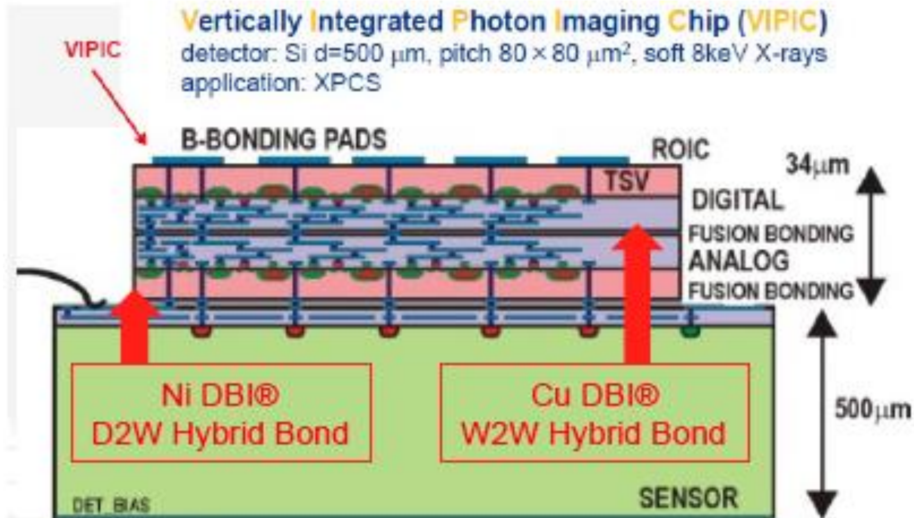
- Communication is limited
  - Data movement costs power
  - Data movement costs time
  - Data movement costs money
  - You can’t aways “phone-home”



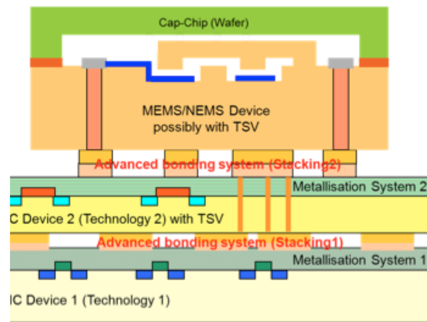
Micralyne



tek-troniks



FermiLab



3DinCites

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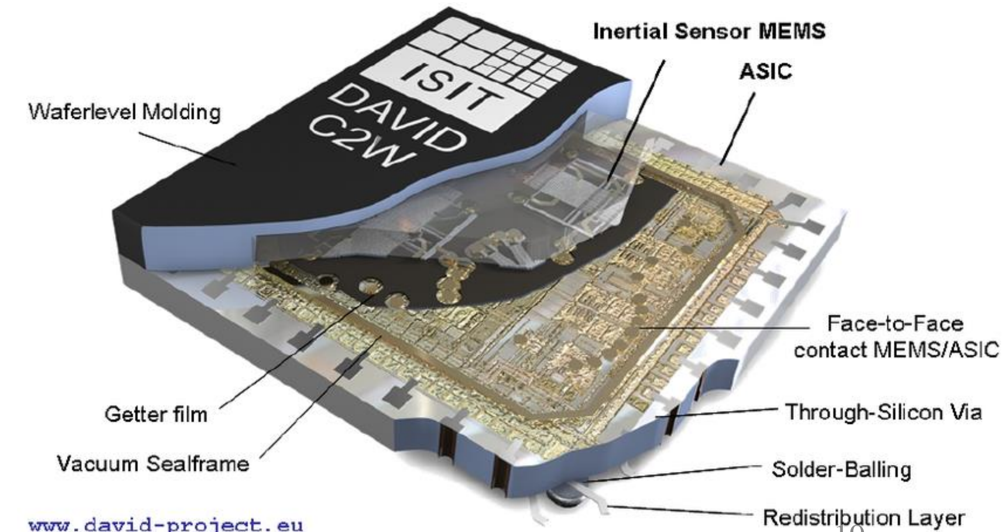
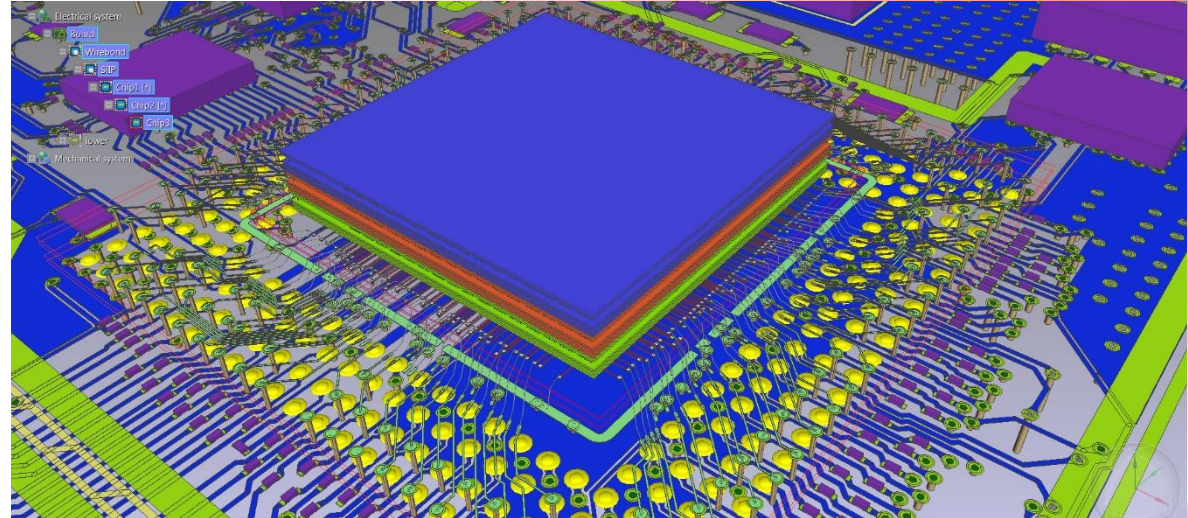
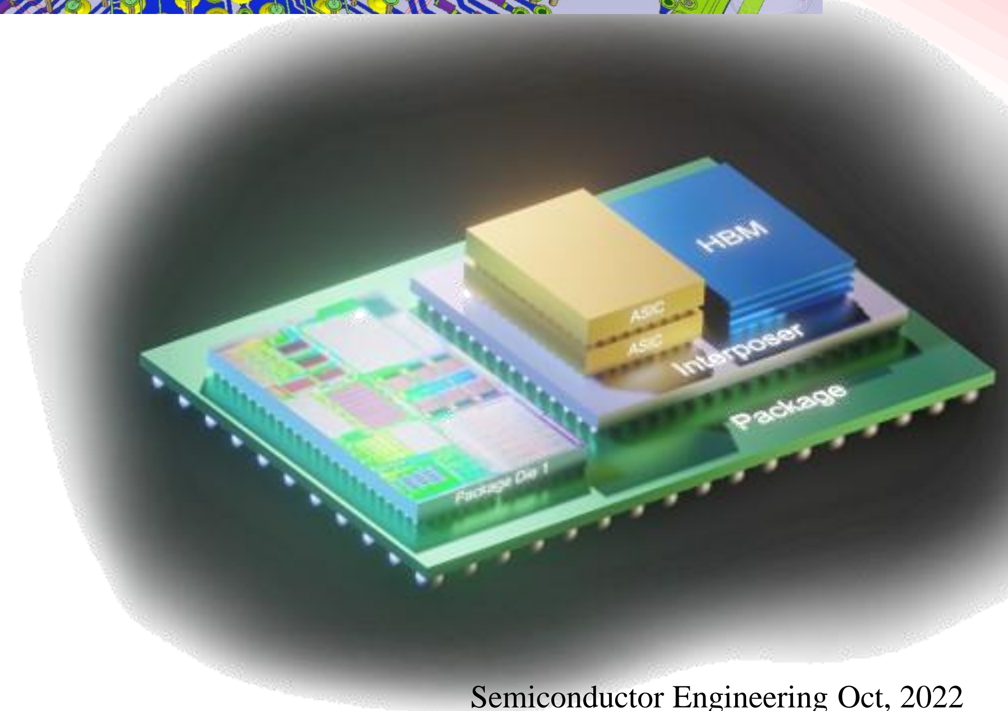


Co-Design and Multi-Physics

- Multi-Dimensional Tools
  - Scale
    - Nanometers to centimeters
  - Electrical
    - Power
    - Signal Integrity
  - Heat
  - Mechanical
    - CTE
    - Modulus
  - Cost
  - Photonics
  - MEMS
  - Liquids

Zuken

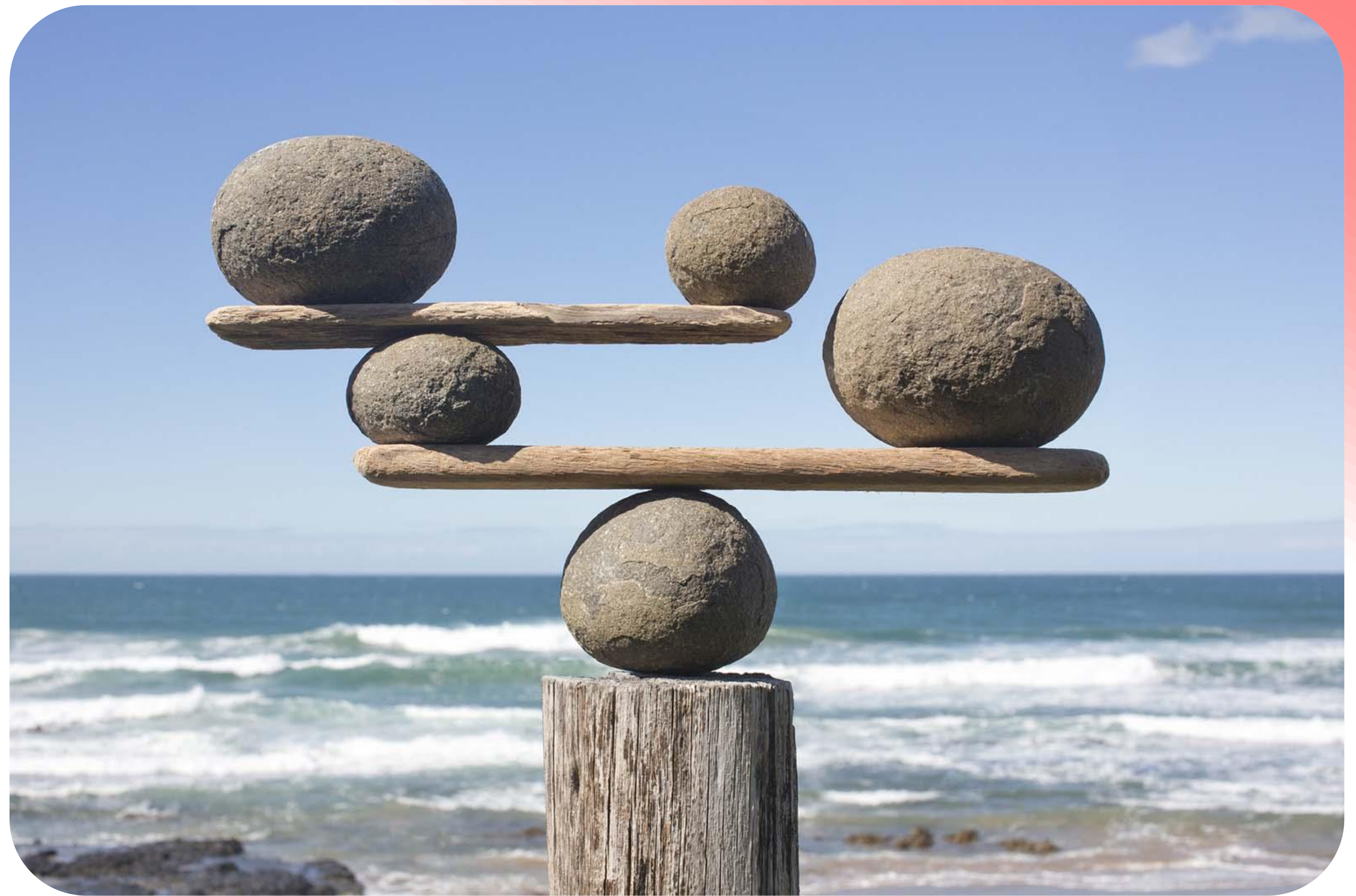




Semiconductor Engineering Oct, 2022

Sensitivities

- PVT
  - Memory
    - 85-95C
  - Logic
    - 85-125C
  - 3/5 Materials
    - GaN @ 400C
  - Sensors
    - 70-175C
  - The more unique materials the greater the complexity



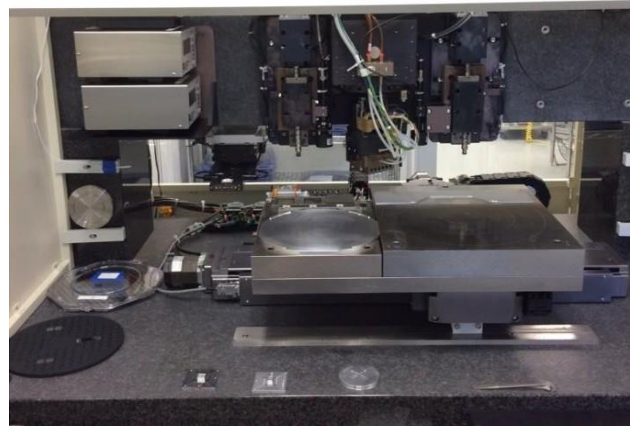
Janus Henderson

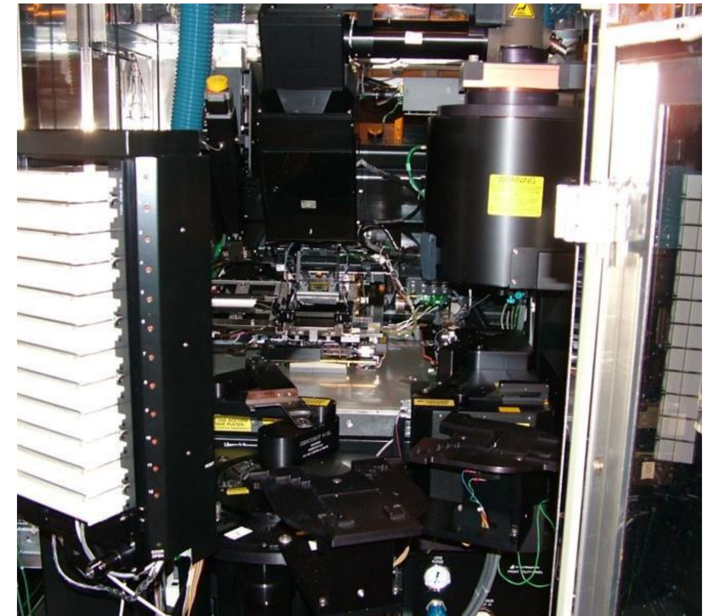
NHanced NC Facilities

The NHanced R&D fab has extensive experience in process development and prototyping, including 2.5D and 3D manufacturing and the use of exotic materials. Its skilled staff has an admirable record of successful projects and a good working relationship with the Naperville design team.

Site capabilities:

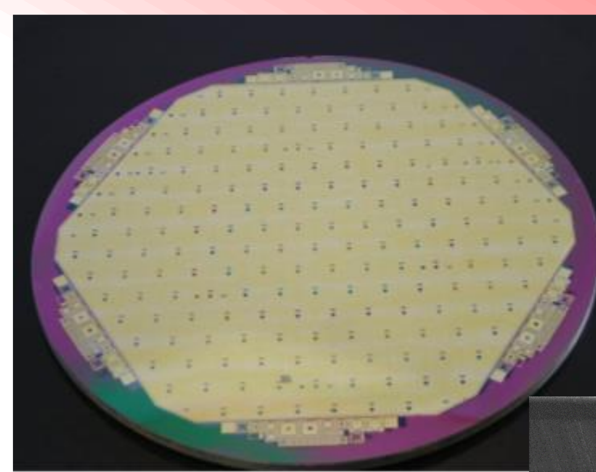
- 25,000 sq ft facility
- 7,000 sq ft clean space (class 100)
- In-house 2.5D/3D technology development
- In-house 2.5D/3D IC prototyping
- Diverse team of engineers and tools to allow operation flexibility
- 100mm, 150mm, and 200mm wafer processing
- Fab processes include photo, etch, metalization, dielectrics, bonding, wafer thinning, and CMP
- Wafer-to-wafer and chip-to-wafer bonding
- ITAR
- ISO 9001-2015
- DMEA TRUST CRADA

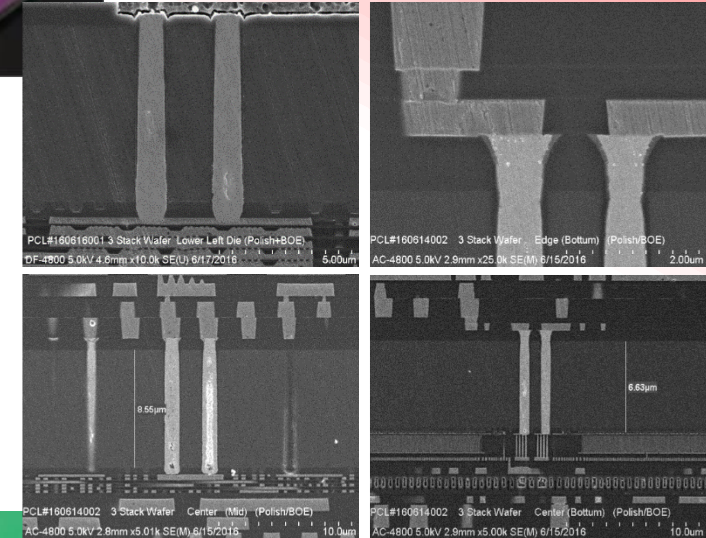




NHANCED SEMICONDUCTORS

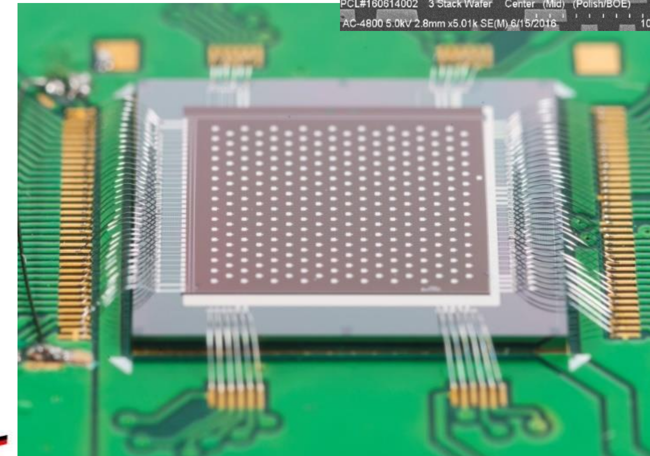
NHanced Small/Medium Scale – High Touch Manufacturing





- 2.5/3D Advanced Packaging
- Si Sensors
- Commercial Development
- Mil-Aero Development and Manufacturing
  - Full BEoL
    - Niche BEoL Processes
    - Cu, Ni, Al, +
  - Split-Fab
  - High k-caps
  - ReRAM
  - 3/5 and LiNbO3 integration
  - Thick Wafer & Thin Wafer Processing
- CRADA in place for Trust

- Target market is customers needing
  1 to 1000 wafers per year

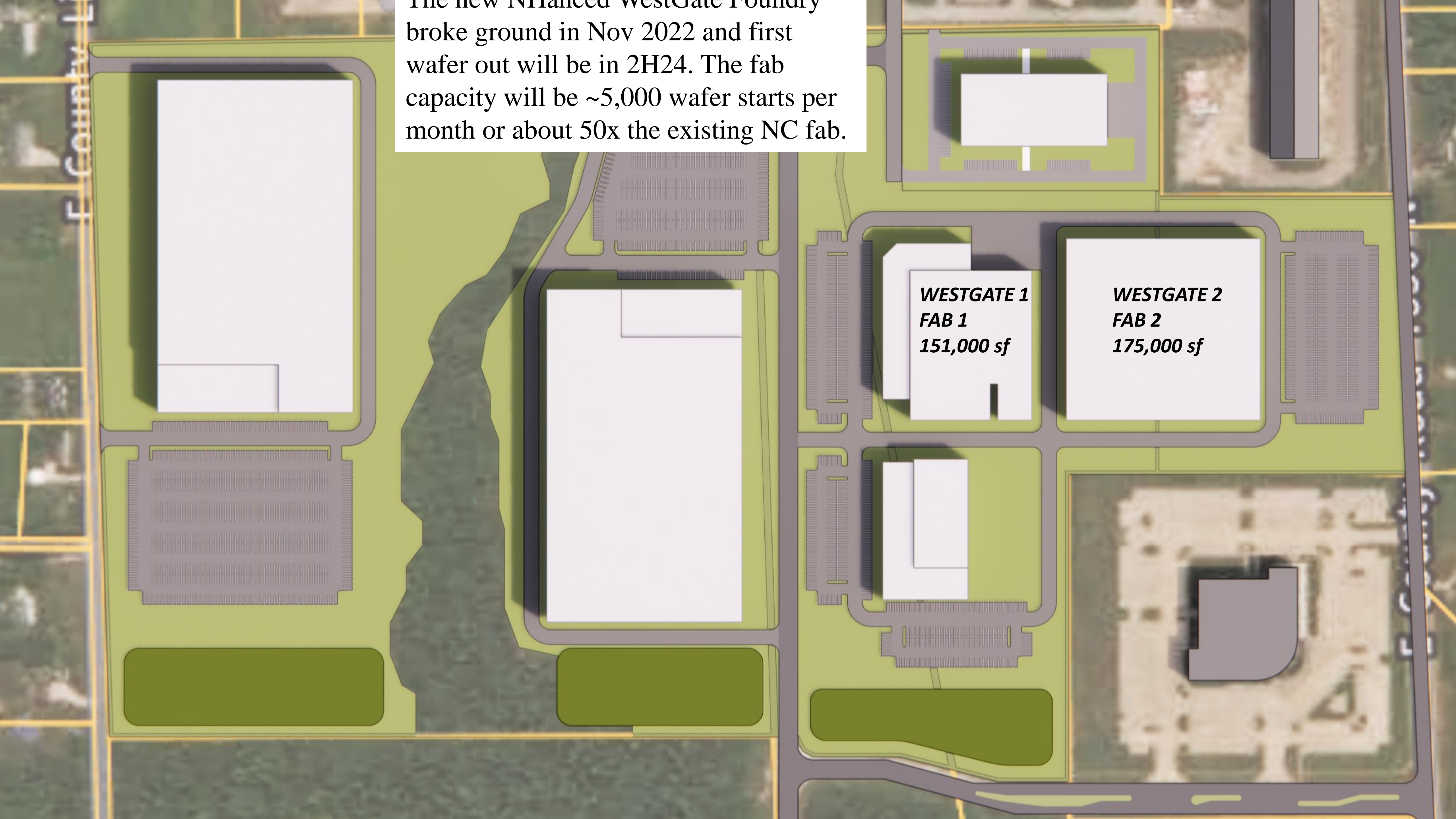


NHANCED SEMICONDUCTORS

Introducing A New "Commons" Manufacturing Model

Cooperative Manufacturing Partnership

NHanced, acting as the managing partner and a neutral entity among foundries and customers provides BEoL and Advanced Packaging services.


The new NHanced WestGate Foundry broke ground in Nov 2022 and first wafer out will be in 2H24. The fab capacity will be ~5,000 wafer starts per month or about 50x the existing NC fab.
WESTGATE 1
FAB 1
151,000 sf
WESTGATE 2
FAB 2
175,000 sf

Provided Commons Capabilities

BEoL processing:

- Adding memory (e.g. MRAM)
- Copper interconnect (down to 22nm tech)
  - Trusted split fab
- RF and power embedded passives
- Full support for 200mm, 150mm, and 100mm

Specialized base materials:

- Interposers: silicon, glass, and fused silica
  - Optical and electrical interconnect
- Advanced substrates: silicon, GaN, GaAs, InP, GaSb, LiNbO3, SiC, etc.

Future support:

- MRAM including strategic Rad Hardened
- 300mm wafer size
- Built-up substrates

Advanced packaging:

- HDI Edge packaging
- Chiplets
- TSV insertion
- Covalent oxide bonding
- Hybrid copper and nickel bonding
  - True heterogenous integration
- Transfer printing assembly
- Wafer reconstitution
- Die-to-die, die-to-wafer, and wafer-to-wafer 2.5D and 3D integration
- Copper pillars
- Wire bonding
- Photonic assembly
- Solder bumping
- Flipchip assembly

Summary – The Road Ahead

- System level Moore's Law future
- Advanced Packaging is driving an industry revolution
  - Enablement of Next Generation Semiconductors
- Advanced Packaging has SWaP+++
  - Ultimately driven by economics

NHANCED SEMICONDUCTORS