Strategic Investment for Innovation: IU’s Contribution to Microelectronics

Dec. 5, 2023

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Home / Stories

Luddy School partnership with NSWC Crane, IEDC to address microelectronics workforce needs

FOR IMMEDIATE RELEASE | Jul 13, 2023

Energy, Vision, Opportunity Fuel Luddy, Loveless Microelectronics Initiative

By: Pete DiPrimio

Sep 22, 2023

With $111M investment, Indiana University betting big on microelectronics

Tuesday, October 10, 2023 12:30 PM EDT
By Peter Blanchard, Indianapolis Business Journal

NEWS • EDUCATION

OCTOBER 13, 2023

IU invests $111 million in microe workforce, research and natio

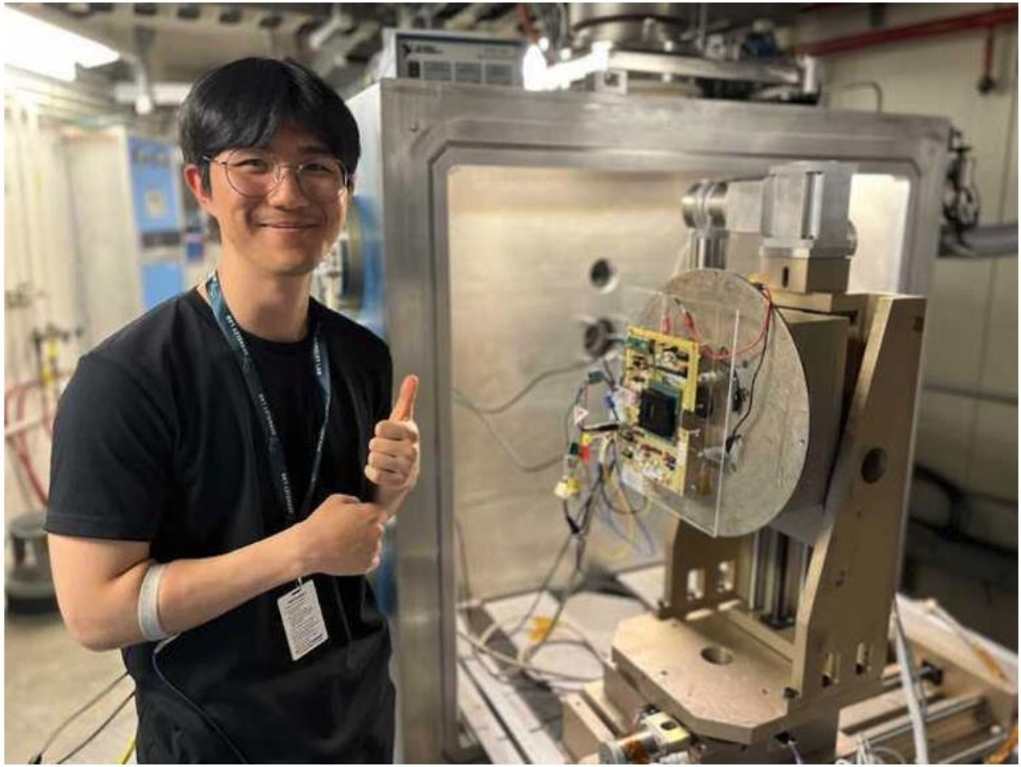
AUBREY WRIGHT -

HIGHER EDUCATION

Indiana University Inv Technology Plan

As part of the federal CHIPS and Sci plan, the university is partnering with tech training programs and industrie

Indiana University's historic partnership with NWSC Crane paves way for microelectronics growth



IU graduate student Jaekon (Jay) Kim stands in front of his experiment at the Lawrence Berkeley National Laboratories 88" Cyclotron Facility in September 2023. IU announced Oct. 10, 2023, it will invest $111 million over the next several years in the microelectronics industry. *Photo by Courtesy Photo / The Indiana*

The Luddy School

3

4

Intelligent Systems Engineering

Established in 2017

Four undergraduate divisions

- Nanotechnology
- Biomedical Engineering
- Computer Engineering
- Cyber Physical Systems

ABET accredited as of 2022

>$40M in research funding since 2017

282 Current students

201 Alumni since 2017

30 Current Faculty

Agenda

Part 1 – The Landscape

- Radiation-Hardened Microelectronics → Resiliency in the face of threats
- The Challenging Path to Trusted Rad-Hard Microelectronics

Part 2 – The Strategy

- Private/Academic/Government partnership for Rad-Hard enablement
- Workforce Ecosystem → It's more than a catch-phrase

Part 3 – A Sampling of Ongoing Research Activities at IU-CREATE

DoD Microelectronics Vision

<u>Vision Statement:</u>

Guaranteed, long-term Access to Measurably Secure Microelectronics

enabling Overmatch Performance

and increasing Military Operational Availability and Warfighter Combat Readiness

This requires a complete solution to be successful…..

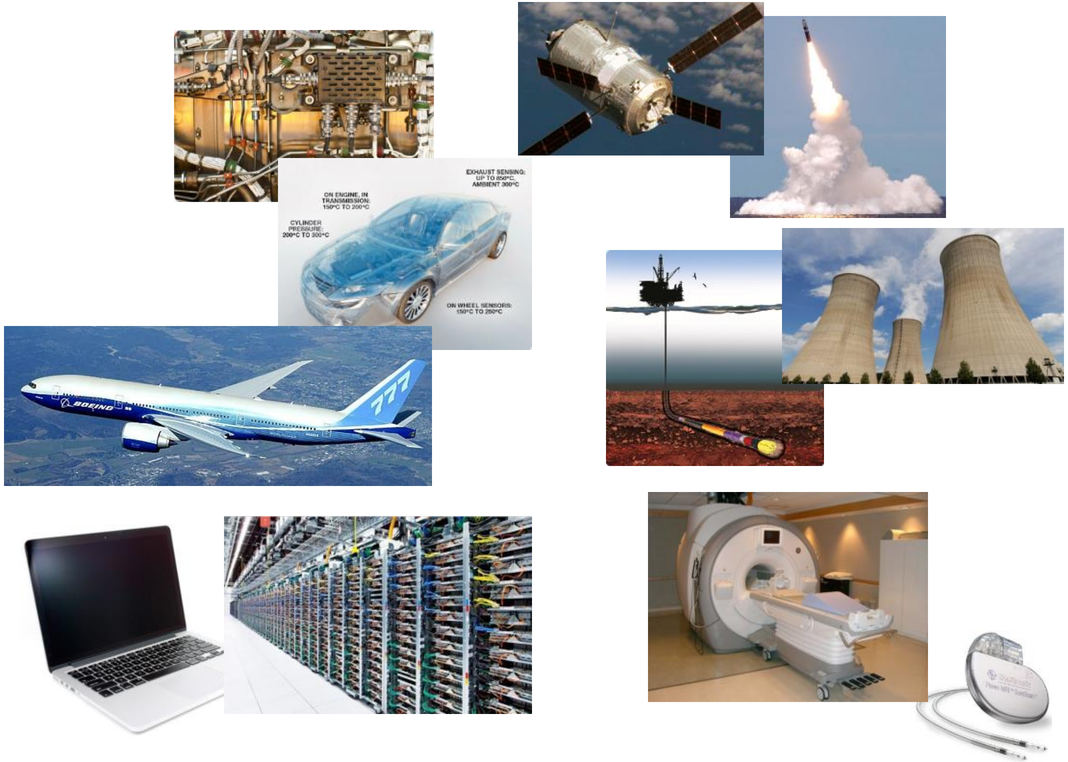
- Ensure timely access to measurably secure and affordable ME technology
- Motivate programs and their primes to modernize and exploit the most capable ME
- Leverage tools, policies and enforcement to reduce or eliminate costly sustainment issues
- Centralize knowledge in a DoD "front door" organization to augment decentralized execution
- Increase ME discovery and innovation, and accelerate transition into DoD systems
- Contribute to and influence interagency and national efforts to grow ME capabilities to meet national security needs
- Cultivate a right-sized workforce with the right skills at the right place and the right time

Mission-Critical Microelectronics

Where failure is not an option:

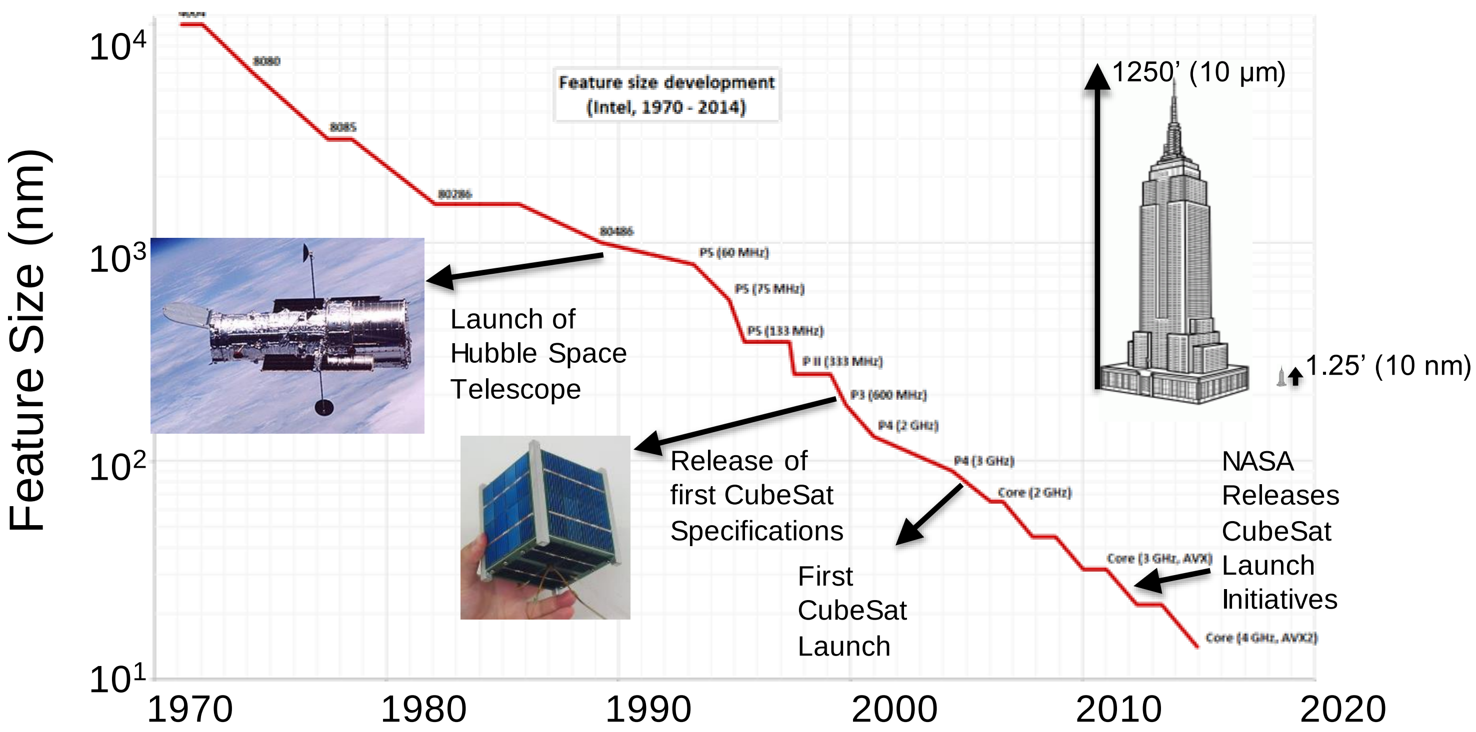
- Mil-Aero/Comm Space
- Nuclear Power
- Weapons
- Medical
- Automotive/Industrial
- High-consequence IT

Harsh environment radiation resiliency is foundational to this ecosystem



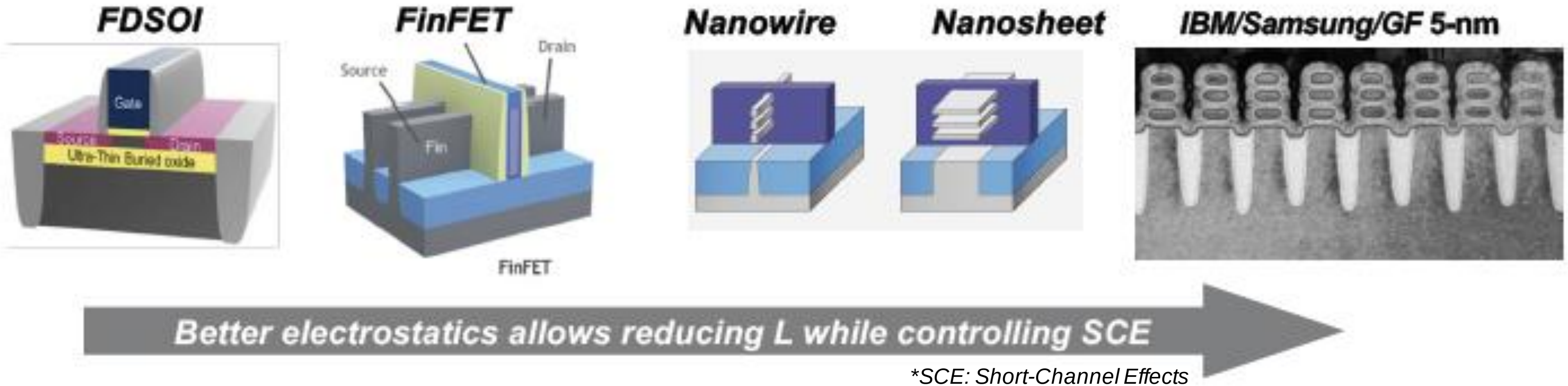
Source: L. Massengill, Rel-Micro

Feature Size Development (Intel)



Source: Intel

Moore than Device Miniaturization



**SCE: Short-Channel Effects*

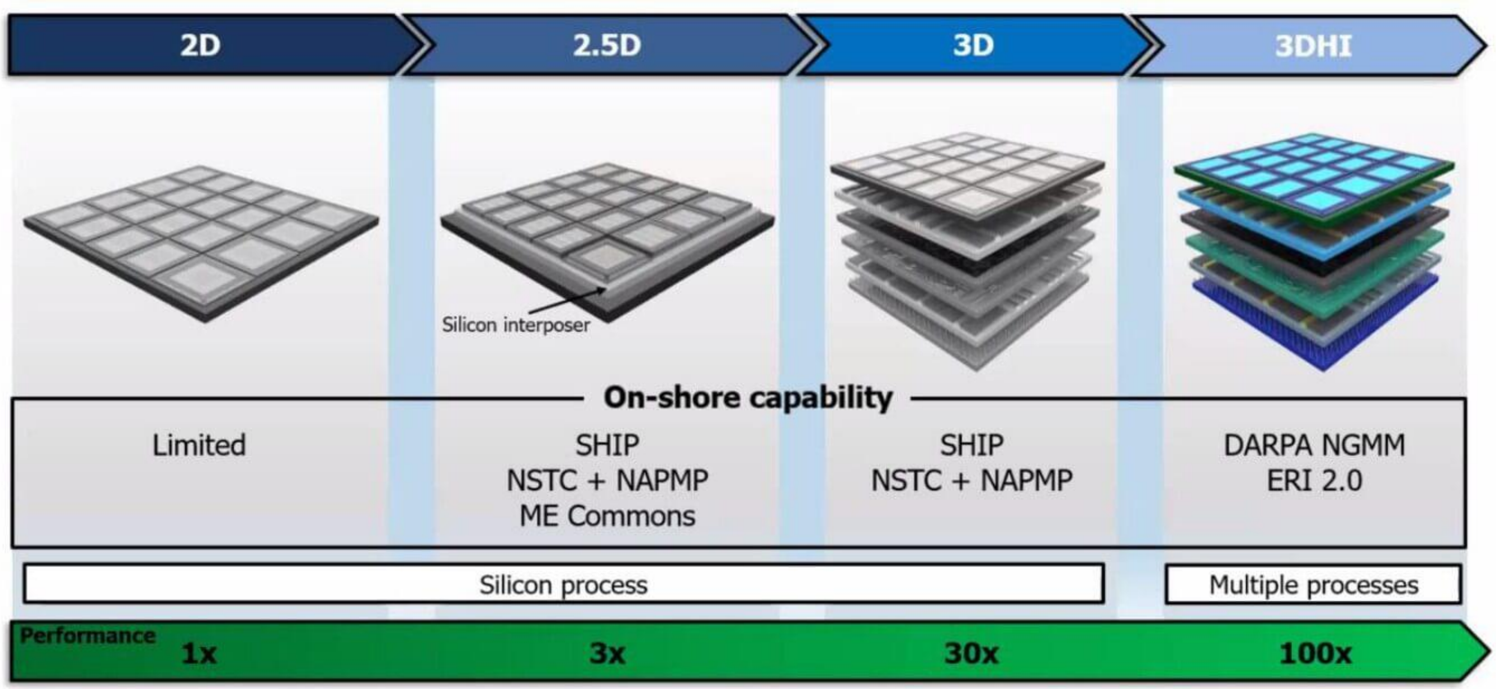
Source: I. Esqueda, JPL Workshop, 2019

Manufacturing Facilities *at the Cutting Edge* are Diminishing

180 nm	130 nm	90 nm	65 nm	45 nm/40 nm	32 nm/28 nm	22 nm/20 nm	16 nm/14 nm	10 nm	7 nm	5 nm
SilTerra										
X-FAB										
Dongbu HiTek										
ADI	ADI									
Atmel	Atmel									
Rohm	Rohm									
Sanyo	Sanyo									
Mitsubishi	Mitsubishi									
ON	ON									
Hitachi	Hitachi									
Cypress	Cypress	Cypress								
SkyWater	SkyWater	SkyWater								
Sony	Sony	Sony								
Infineon	Infineon	Infineon								
Sharp	Sharp	Sharp								
Freescale	Freescale	Freescale								
Renesas (NEC)	Renesas	Renesas	Renesas	Renesas						
Toshiba	Toshiba	Toshiba	Toshiba	Toshiba						
Fujitsu	Fujitsu	Fujitsu	Fujitsu	Fujitsu						
TI	TI	TI	TI	TI						
Panasonic	Panasonic	Panasonic	Panasonic	Panasonic	Panasonic					
STMicroelectronics	STM	STM	STM	STM	STM					
HLMC	HLMC		HLMC	HLMC	HLMC					
IBM	IBM	IBM	IBM	IBM	IBM	IBM				
UMC	UMC	UMC	UMC	UMC	UMC		UMC			
SMIC	SMIC	SMIC	SMIC	SMIC	SMIC		SMIC			
AMD	AMD	AMD	GlobalFoundries	GF	GF	GF	GF			
Samsung	Samsung	Samsung	Samsung	Samsung	Samsung	Samsung	Samsung	Samsung	Samsung	Samsung
TSMC	TSMC	TSMC	TSMC	TSMC	TSMC	TSMC	TSMC	TSMC	TSMC	TSMC
Intel	Intel	Intel	Intel	Intel	Intel	Intel	Intel	Intel	Intel	Intel

Source: https://en.wikichip.org/wiki/technology_node

Manufacturing Capabilities Are Stacking Up



Source: DARPA

Radiation Effects Engineering

Radiation Environments

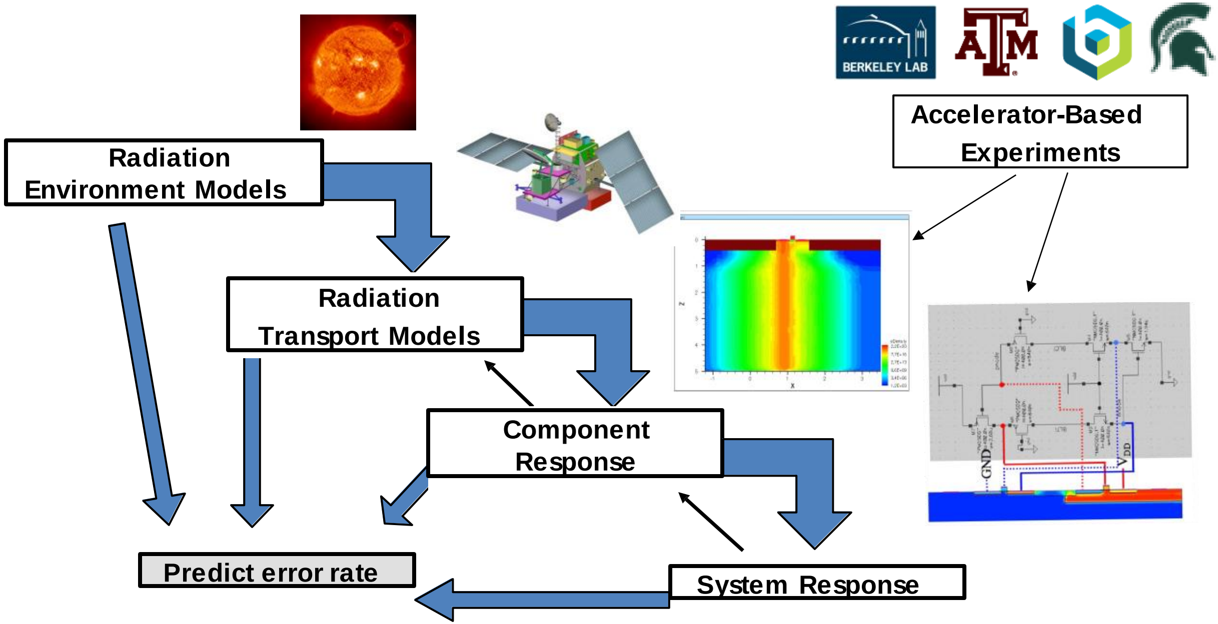
- External Space
- Transport Dose / Flux

Component Response

- Total Ionizing Dose
- Displacement Damage
- Single Event Effects
- Prompt Dose Effects

Sub/System Reliability / Availability

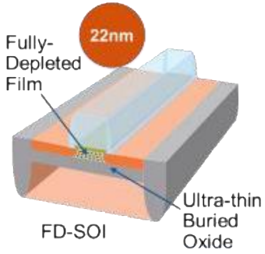
- Worst-Case Analysis
- Probabilistic Analysis

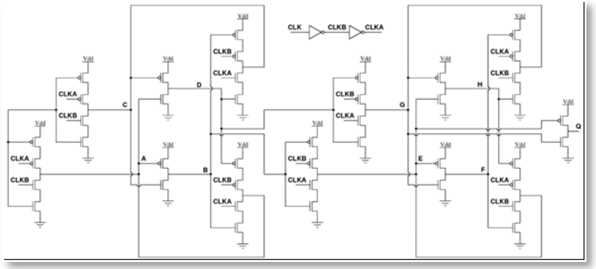


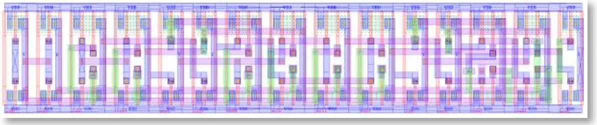
Radiation Hardening 101

Multiple approaches may be employed (independently or in combination) to protect electronic systems

- Radiation Hardened by Process (RHBP)
  - Specific materials/layers/wafers (e.g. SOI), processing techniques
  - Examples: UTBB/SOI, dielectric engineering
  - Most appropriate for TID, SEL
  - Usually requires a dedicated rad-hard foundry fabrication line ($$$)
  - Only viable business model: U.S. government support
- Radiation Hardened by Design (RHBD)
  - ASIC chip layout or circuit modifications for charge isolation and/or information redundancy (spatial & temporal partitioning)
  - Examples: DICE cell, guard gate, interleaved layout
  - Most appropriate for SEU and SET
  - Requires rad-hard IP + fabless ASIC flow + pure-play foundry ($$)
  - DoD and 'old' space interest and support
- Radiation Hardened by Architecture (RHBA)







Source: L. Massengill, Rel-Micro

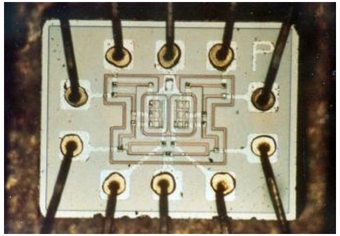
Challenges for Radiation Hardening

The Big Picture

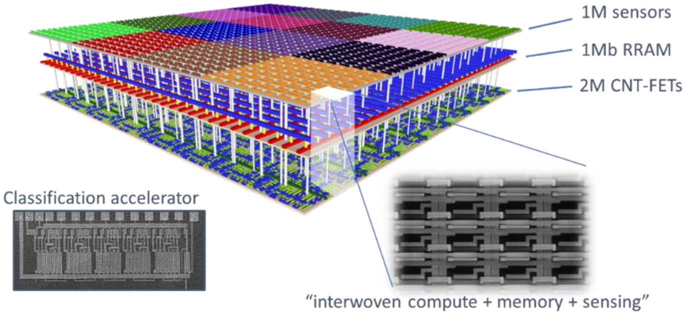
- State-of-the-art chip systems contain billions of transistors, integrated analog and digital, 3D IC stacks, and multiple voltage domains
- Critical charge can be just a few fC

Challenges for RHBD

- Integration of process, layout, topology, and system-level approaches
- Architecture-level SE simulation and high-level RHBD approaches
- SEE for low-power circuits
- Development and analysis of RHBD libraries
- Integrated modeling, simulation and experimental analysis methodologies for advanced technology ICs

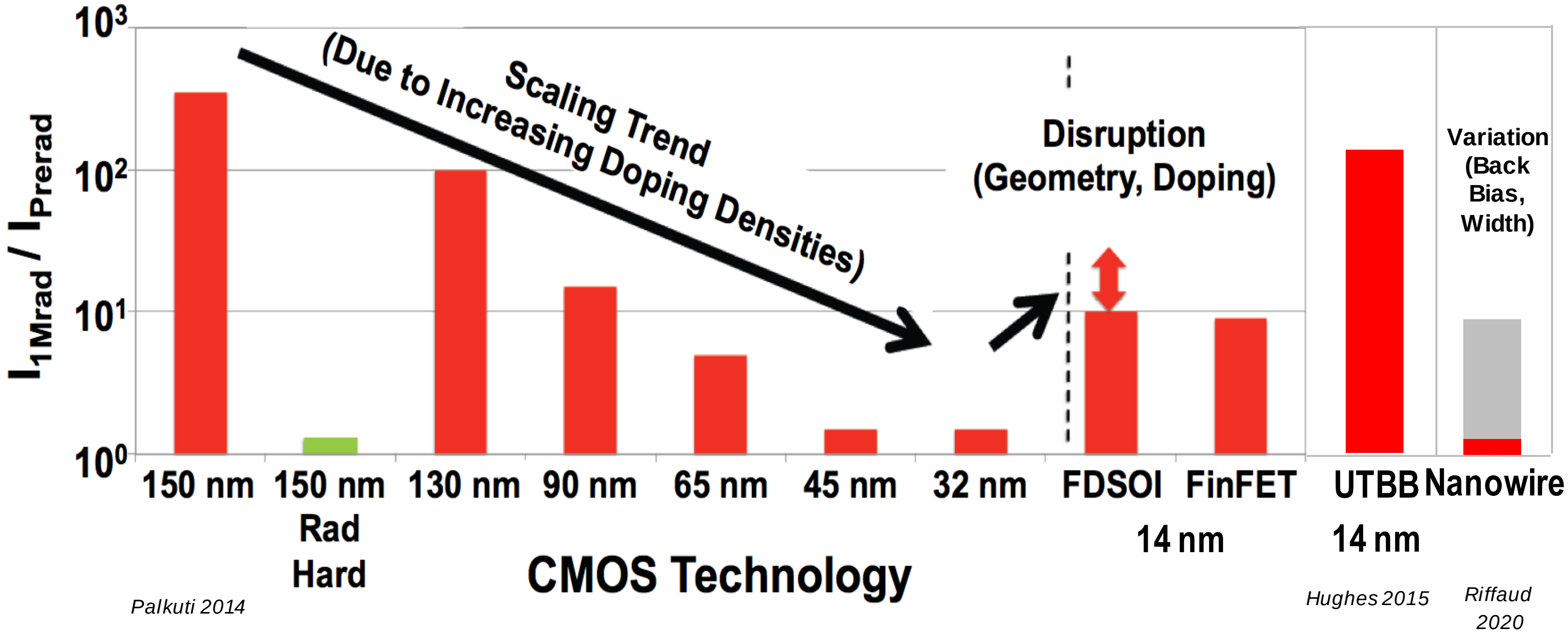


Logical NOR IC from Apollo (~1961)



3D-SoC sensor/machine learning IC from Stanford (2017)

Good for Job Security, Challenging for Assurance



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Technology is Evolving Rapidly, So Must Education and Workforce

By 2030 …

300,000

Shortage of engineers

90,000

Shortage of skilled workers

Source: https://www.mckinsey.com/industries/semiconductors/our-insights/how-semiconductor-makers-can-turn-a-talent-challenge-into-a-competitive-advantage

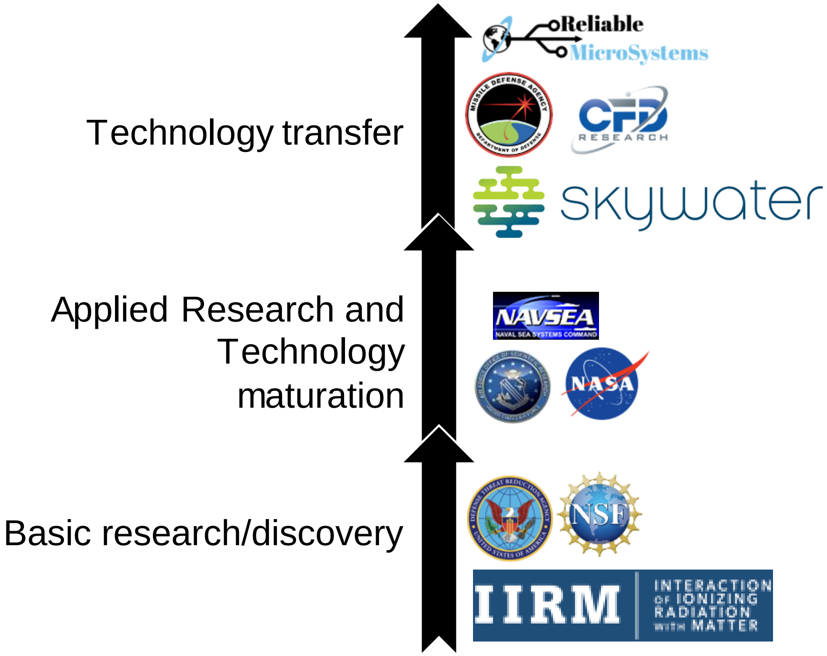
Process vs **Ecosystem**

Process:
- Multiple participants with well-defined roles
- Designed for an end customer
- Participants may have different interests but work towards shared goal
- Repeatable, predictable, and measurable outputs
- Regular paths to uniform outputs

Ecosystem:
- Multiple participants with **diverse roles**
- **Naturally evolves** to meet diverse needs of all participants
- Participants may have different interests and sometimes even competing interests
- Evolving outcomes and **adaptation to changing circumstances**
- Diverse paths to variable outcomes, even for similar participants

Source: deloitte.com/insights

Funding Diversity



Current grants & contracts:

- SCALE OUSD/T&AM
- IEDC
- CFDRC (MDA P2 STTR)
- SkyWater
- DTRA IIRM (PSU)
- SCALE WFD
- NASA
- Nimbis Services (MDA)
- CFDRC (DTRA P1 SBIR)
- CFDRC (NASA P2 SBIR)

$3.5M in Expected FY24 Research Expenditures

IU's investments in microelectronics include:

- Faculty 100 hiring initiative, investing $23.5 million over the next five years to recruit 25 new faculty members in microelectronics, nanotechnology, artificial intelligence, machine learning and cybersecurity. **IU will focus on hiring faculty with Department of Defense experience**, as well as the creativity and entrepreneurial ability to develop **dual-purpose technologies** and capabilities.

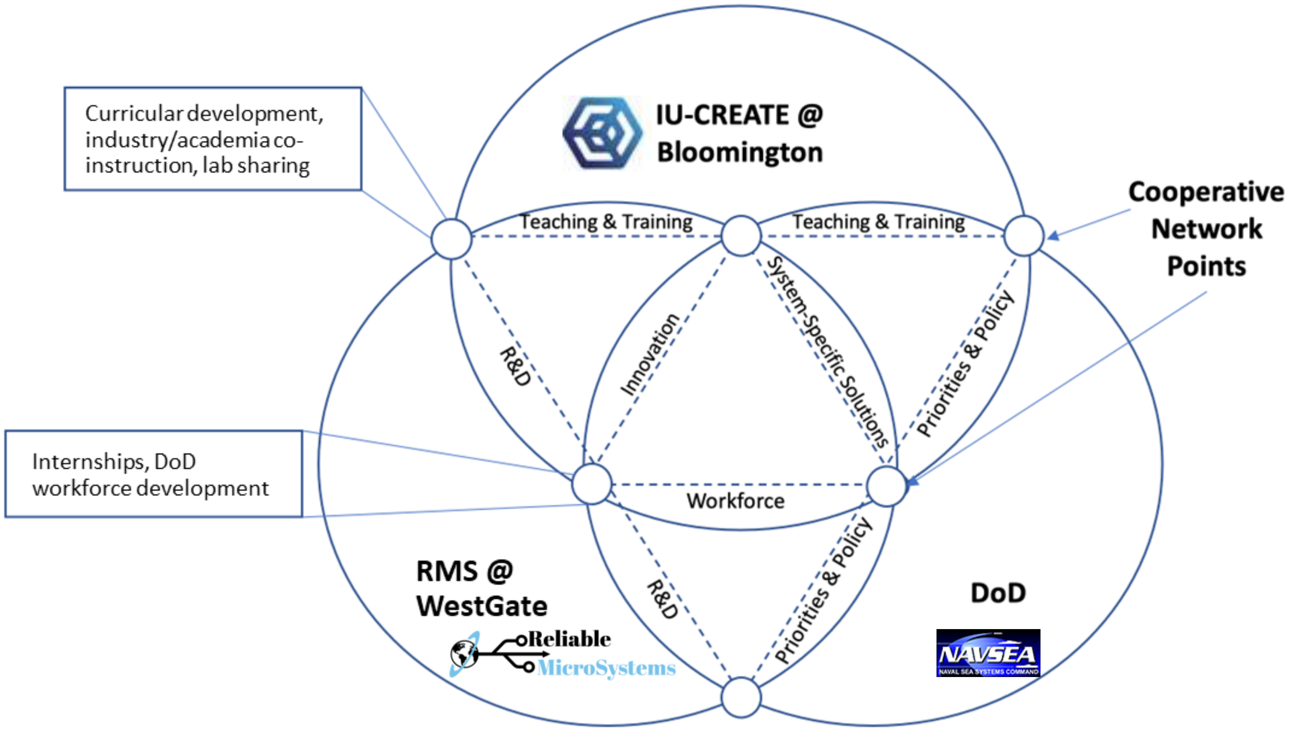
- Investing $53.5 million in **laboratories and other facilities**, equipment and faculty start-up costs to support key research areas with defense applications; increase research partnerships; expand federal grants and contracts; and create additional opportunities for IU and Crane personnel to collaborate.

- Announcing today a $10 million investment to launch the new Center for Reliable and Trusted Electronics, which will lead research activities focused on the modeling and simulation of radiation effects and the design of radiation-hardened technologies. The center, to be known as IU CREATE, will build on an existing initiative at the IU Luddy School of Informatics, Computing and Engineering supported by a $5 million grant from NSWC Crane and an additional $1 million from the Indiana Economic Development Corp. that is focused on **building and testing microelectronics in extreme environments**.

- Implementing new degree programs to train students in microelectronics and nanofabrication and investing in nanofabrication facilities to support IU programs and the IU-NSWC Crane partnership. The total developmental, renovation and equipment, and operational commitment will be $13.5 million.

- Committing $1 million for each of the next five years to support innovative faculty research in key technology areas such as biotechnology and synthetic biology.

Early Construction – IU/RMS/Crane Team



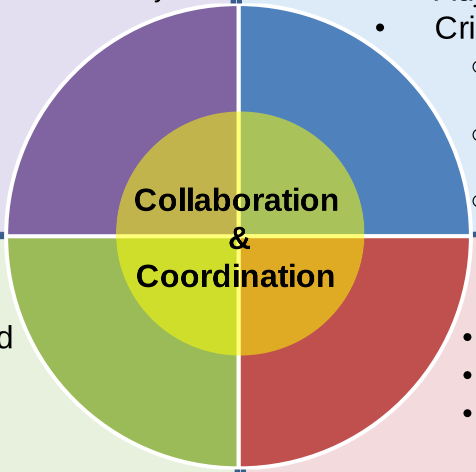
IU Center for REliable And Trusted Electronics

Community of Policy & Practice

- Working group of academic, DIB, and government experts
  - Track barriers, opportunities, and policy priorities for entry into semiconductor manufacturing and microelectronics design
  - Assess technology and workforce readiness
  - Provide export regulation expertise to drive reform

Research & Development

- Extreme environment & dual use technologies
- Adjacent commercial markets, e.g., automotive
- Critical infrastructure
  - Diverse funding and integrated research and technology maturation
  - Leading-edge computational and experimental capabilities
  - Shared resources, e.g., Westgate, DIB

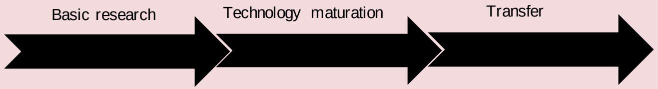


Workforce Development

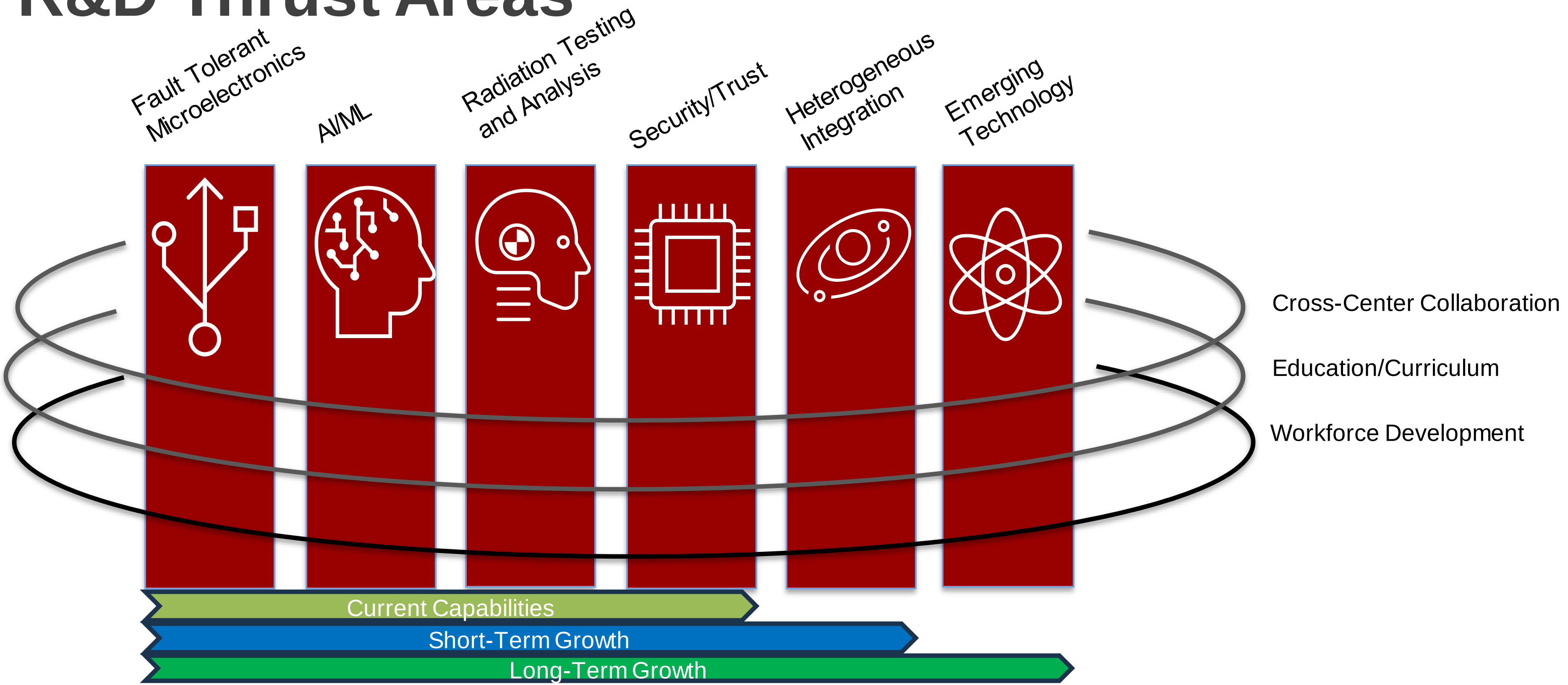
- Provide a ready workforce for RH design and test through interactive academic-industry-government partnership and cooperative network for teaching/training, R&D, and development of policy guidelines
  - Mentorship programs
  - Internship placements
  - Certifications

Trust & Assurance

- Technology readiness
- Mission-driven solutions
- Verification and validation



R&D Thrust Areas



Innovation in RH Education and WFD

SCALE
SCalable Asymmetric Lifecycle Engagement

Applied Abilities	Workforce Placement, Tech. Transfer
Industry Collaboration	Internships, Training, Export Control
Guided Research	R&D/Applied Skills
Knowledge	Curriculum and Certification Units
Early Exposure	Practical Skills Modules

(1) STEM:
- Pre-collegiate and community college programs
- Certificates and learning modules
- Apprenticeships

(2) Undergraduate Coursework:
- New courses on Extreme Engineering, Creative Design, Semiconductor Devices, Intro to Radiation Effects, and Systems Engineering

(3) Graduate Coursework:
- Courses in radiation effects (Radiation Effects and Reliability, Embedded Systems for Space Applications)
- Opportunities for specialty electives

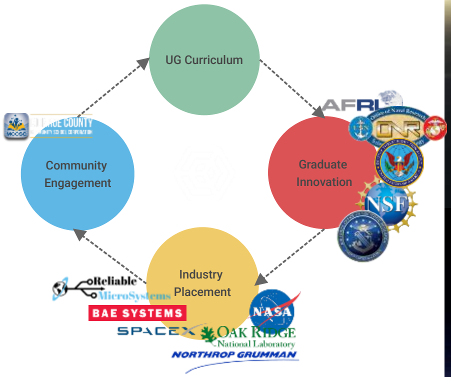
(4) University-Sponsored Projects:
- Experiential learning credited coursework
- UG/GA research
- Sponsored capstone design
- Community engagement

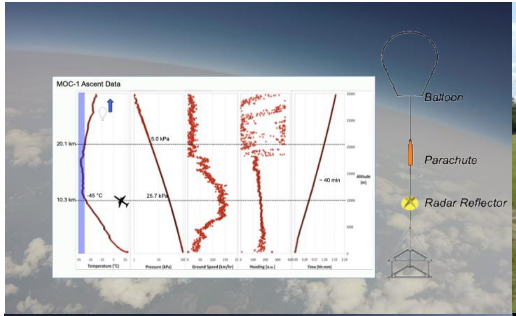
(5) Networking Outreach:
- Wide community-based network and technology ecosystem
- Industry involvement, training and workshops
- Mentorship programs
- Career and networking fairs

Experiential Learning

SCALE
SCalable Asymmetric Lifecycle Engagement

- ENGR-E 399/599: Microelectronics Radiation Effects and Reliability
- ENGR-E 490: Capstone Summer Research Experience for Undergraduates
- ~20 undergraduate/graduate student researchers per year





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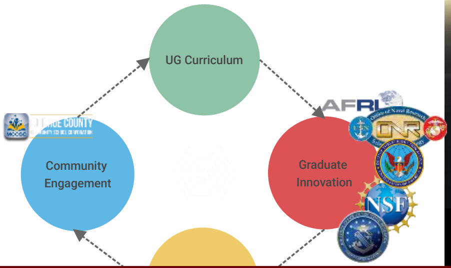
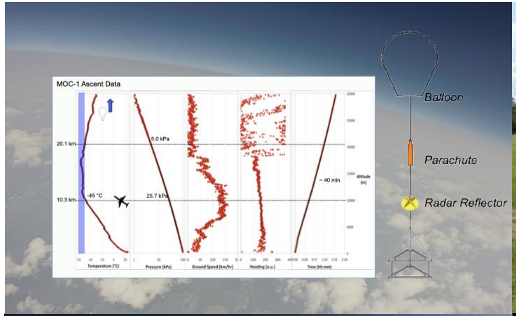
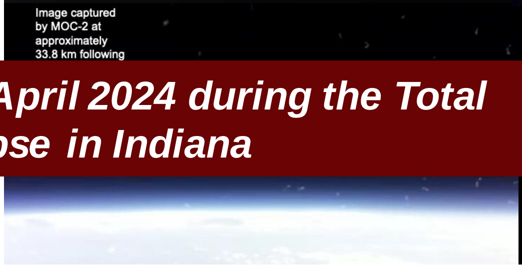






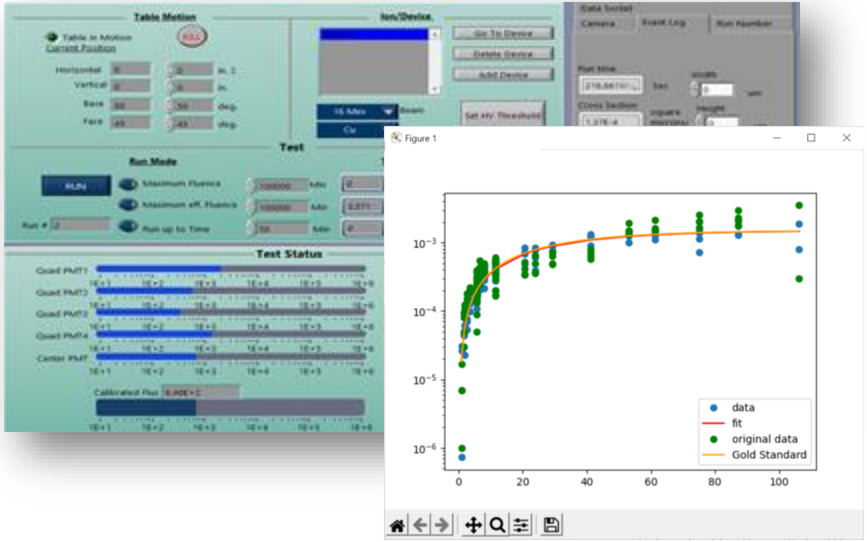
IUB-Sat will launch in April 2024 during the Total Solar Eclipse in Indiana

Industry-Relevant Capstone Experiences

SCALE
SCalable Asymmetric Lifecycle Engagement

ISEEU Heavy-Ion Scheduler Currently Being Delivered to MDA for use in DeCPTR

LBNL Emulator to be used in collaboration with Vanderbilt LabRaTTS



Industry-Relevant Capstone Experiences

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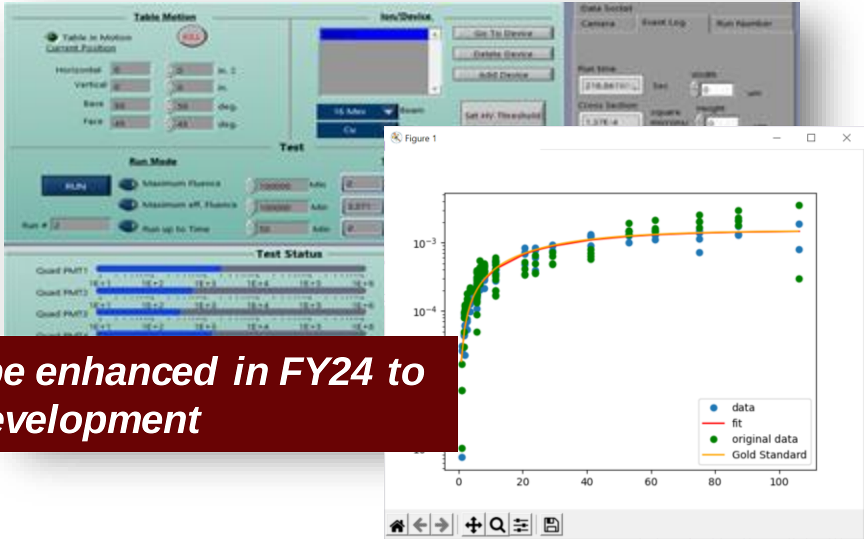

ISEEU-Smart Scheduler will be enhanced in FY24 to aid in test plan development

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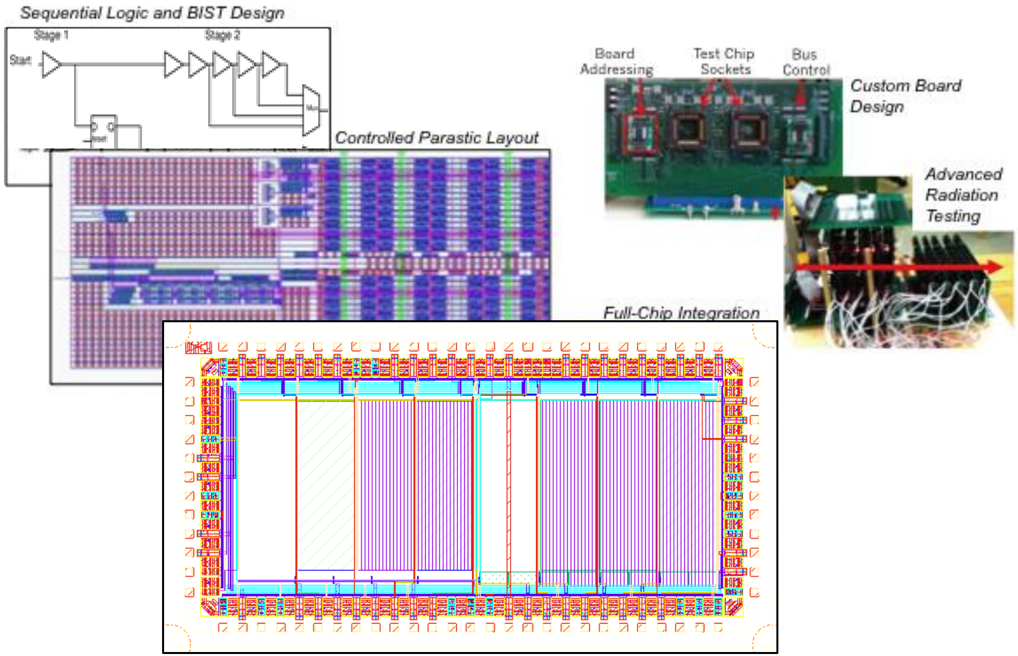
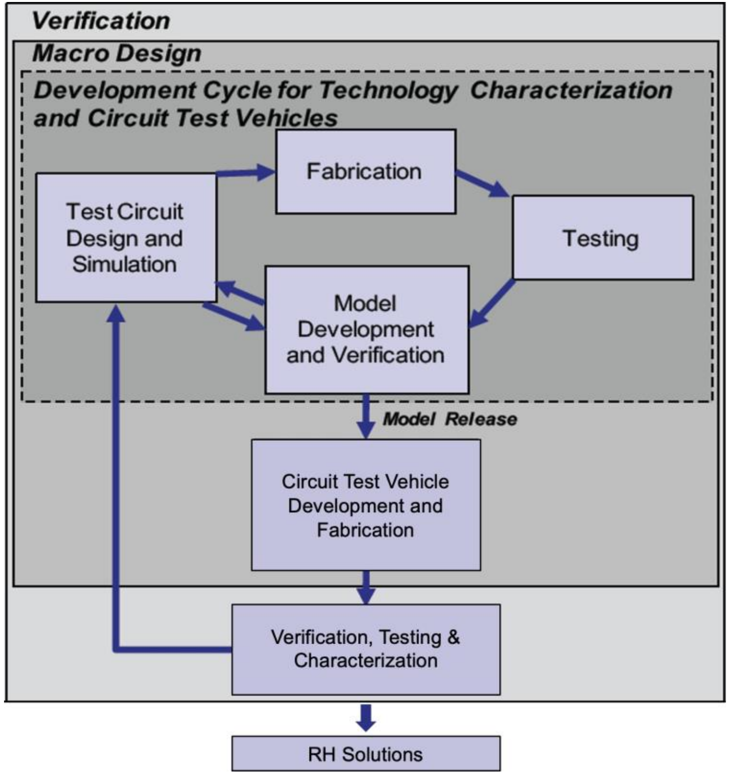
End-to-End: IC Design, Fab, and Test

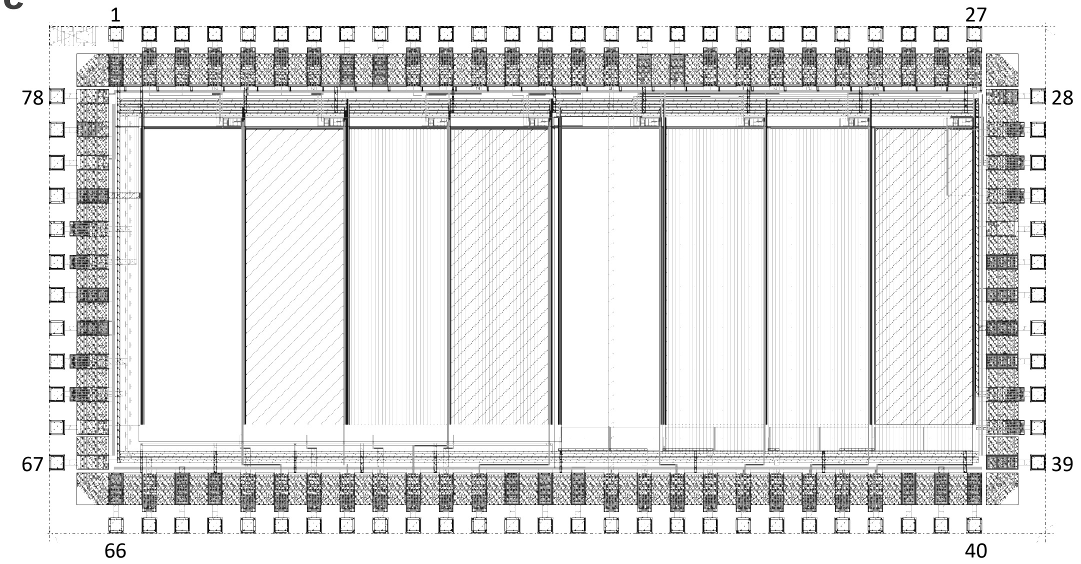




Example Project (Nisswa):

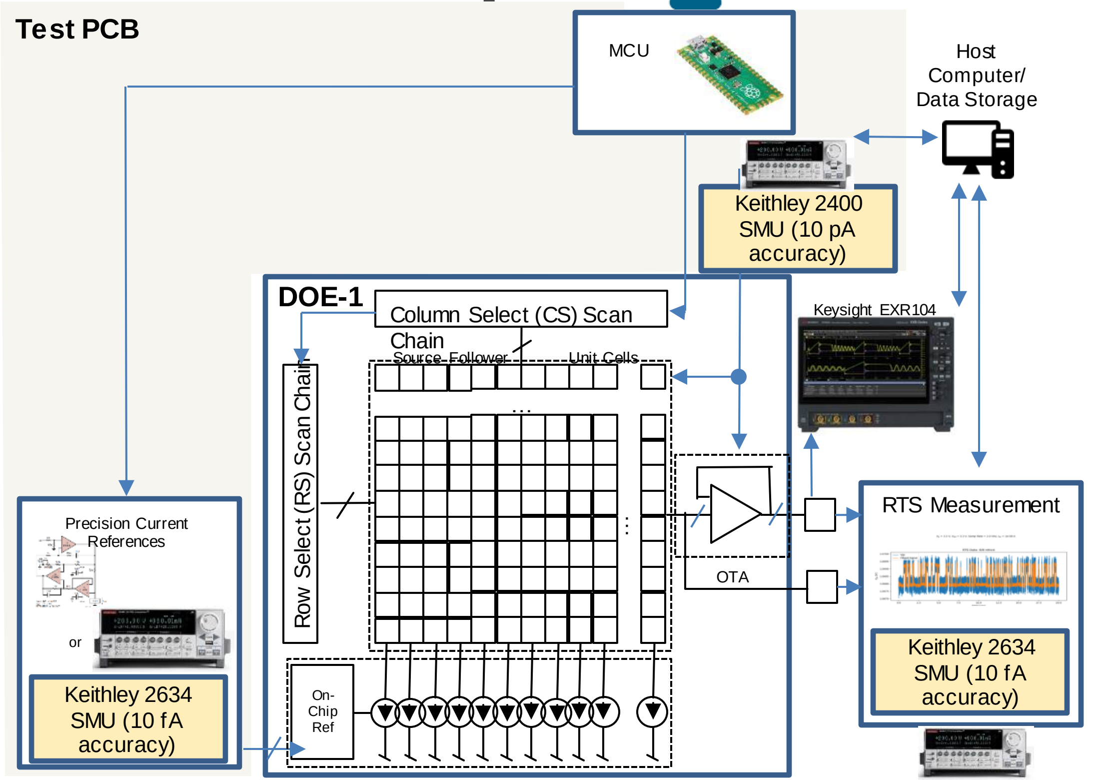
On-Chip Characterization of RTS Noise

- Framework for large-scale random-telegraph signal (RTS) characterization of SkyWater S90LN
- The focus is on improving spatio-temporal statistics
- DOE1-C3:
  - 90nm bulk CMOS
  - built-in-self-test (BIST) architecture for on-chip measurement of RTS of a large transistor array (~2x10^{4} transistors – 256x96)

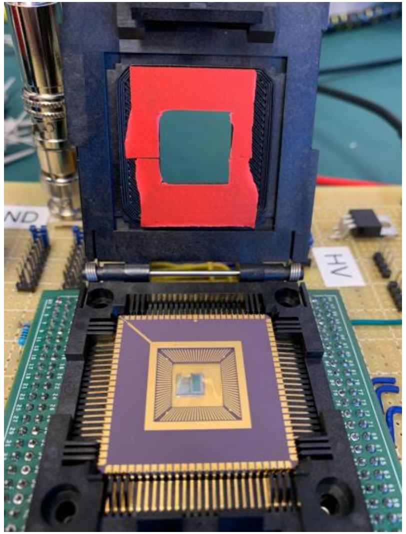


DOE1-C3 On-Chip RTS Test Setup

- 24,576 unit cells accessed via row and column scan chains controlled by an external MCU
- Unit cells comprised of **all transistor variations available in technology** at 8 W/L ratios per type and deep n-well option

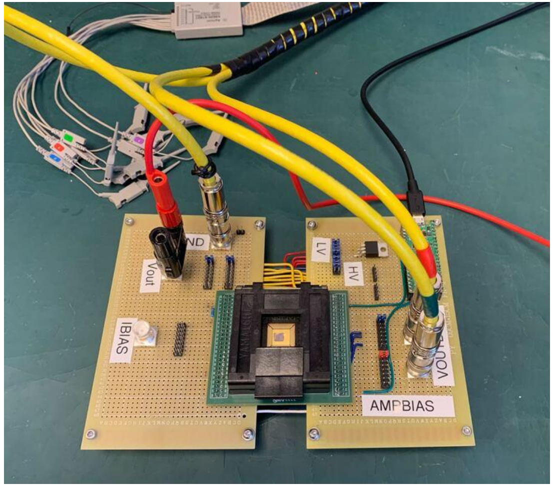


DOE1-C3 On-Chip RTS Test Setup



DOE-1 Chiplet 3 Packaged in 100 LCC
on Custom Daughter Card

Chips labeled DOE1-3-*N*

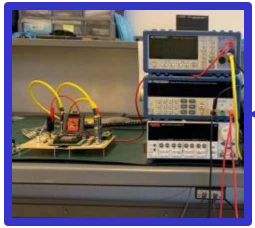


Final Test Board for RTS Measurement (P2.0)

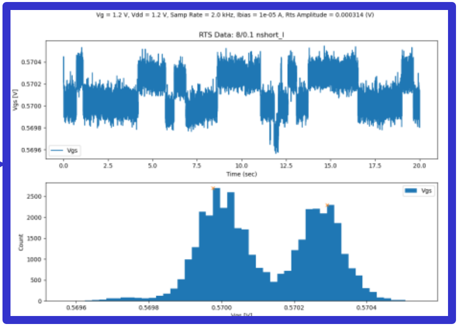
Prototype Test Board for RTS Measurement (P1.0)

DOE1-C3 On-Chip RTS Test Setup

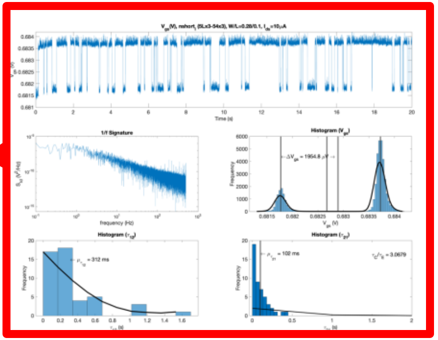
skywater



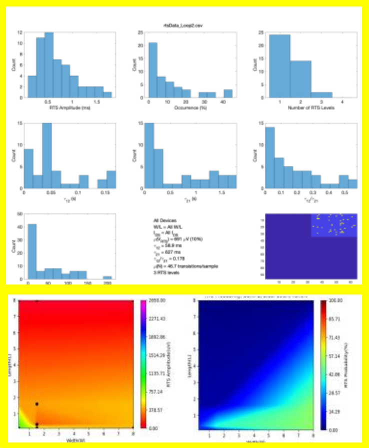
Pre-process/Initial Scan



Data Processing

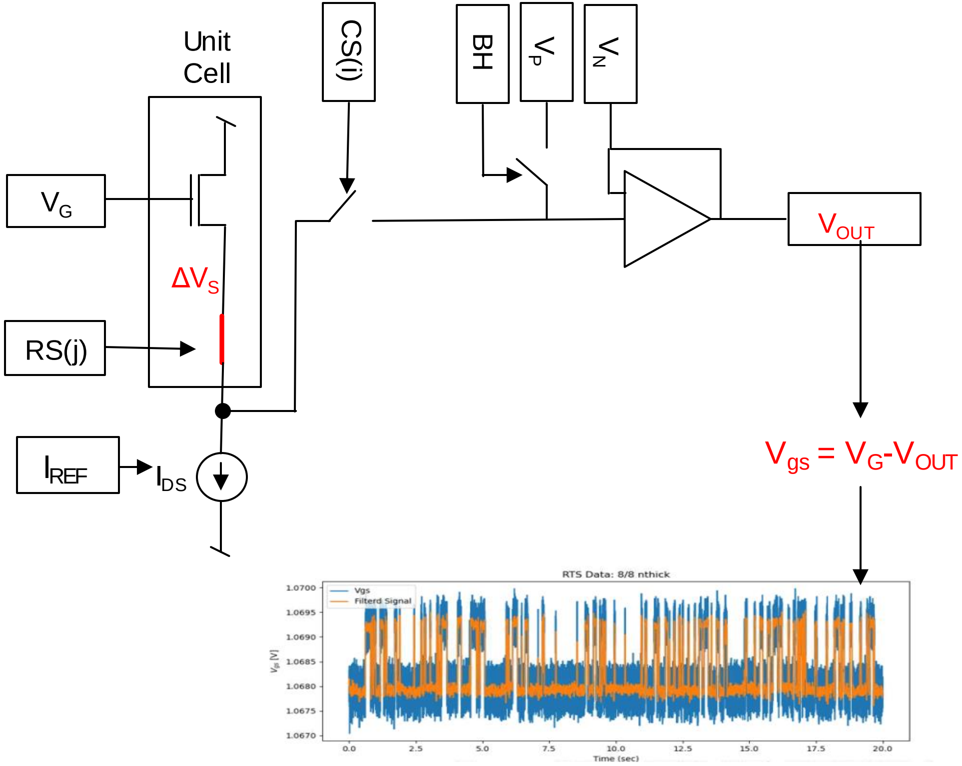


Statistical Analysis



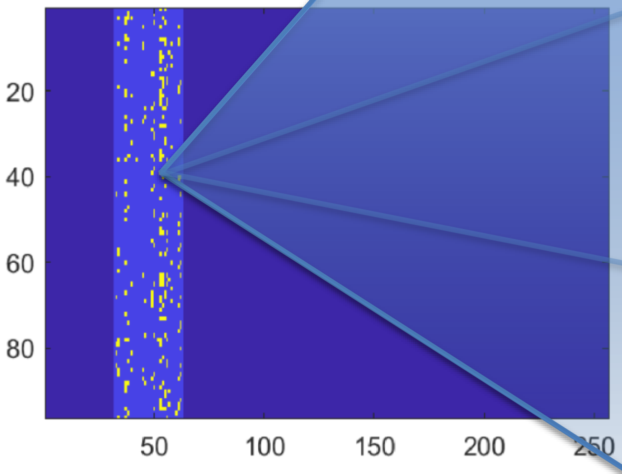
DOE1-C3 On-Chip RTS Measurement

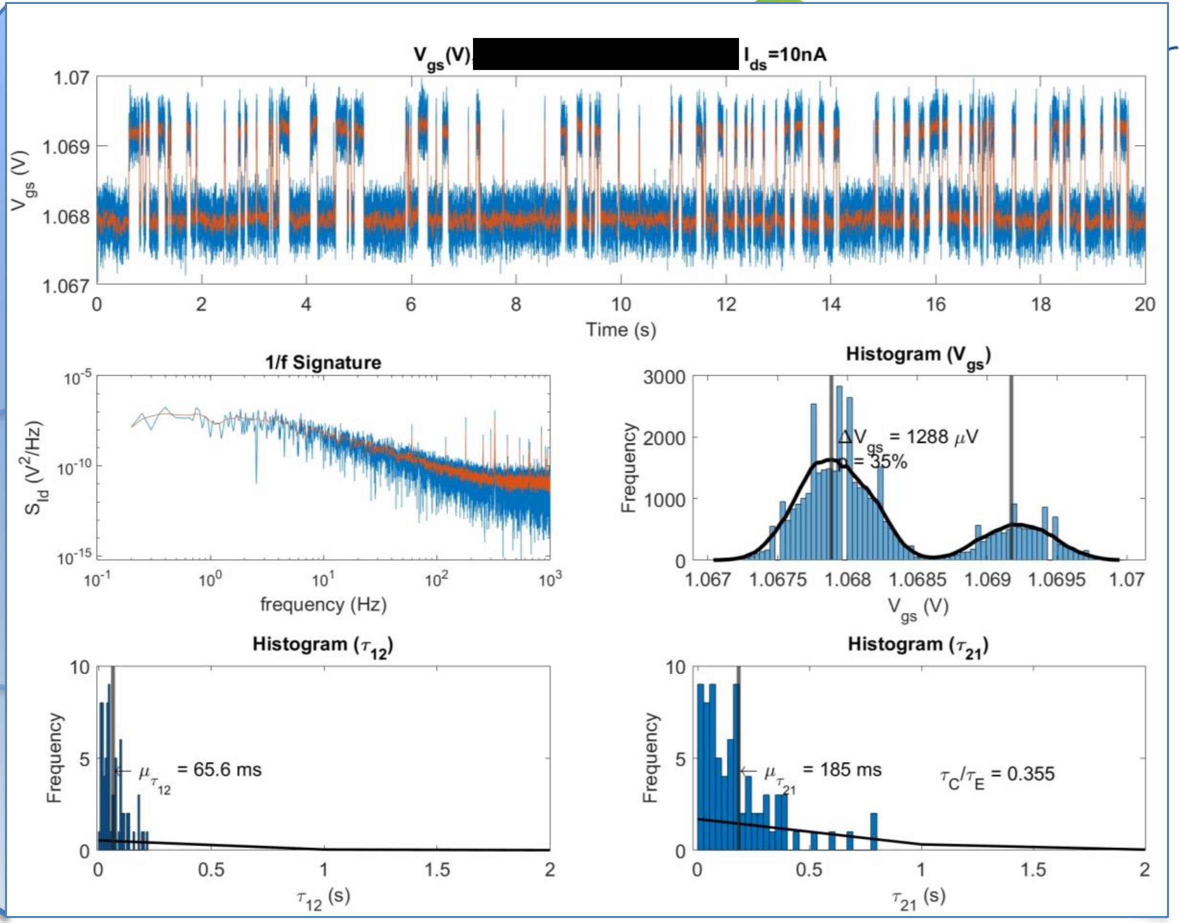
- The device under test (DUT) within each Unit Cell is biased as a source follower using an on-chip current source (I_{DS}) and an externally applied gate bias (V_G)
- ΔV_S is measured via an on-chip amplifier, thus allowing for extraction of ΔV_{GS}
- RTS manifests as discrete shifts in V_{GS}
- Capture (τ_C) and emission (τ_E) time constants, and other statistical parameters are measured



Example of 2 Level RTS

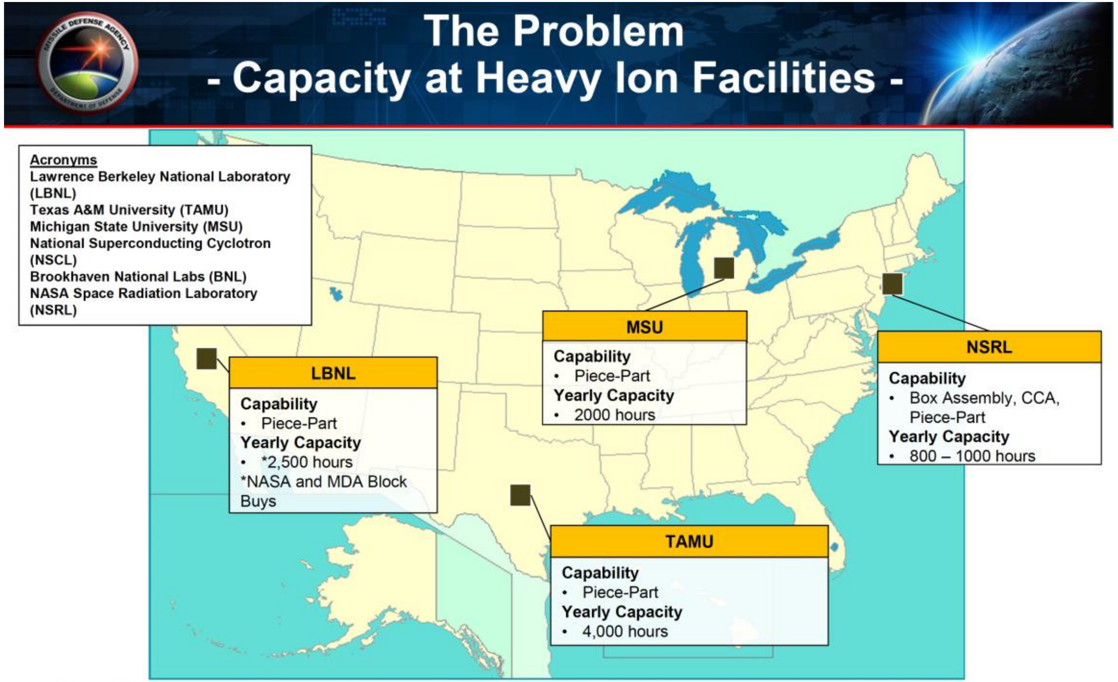
-DEVICE TYPE OBFUSCATED-





Next … Radiation Testing

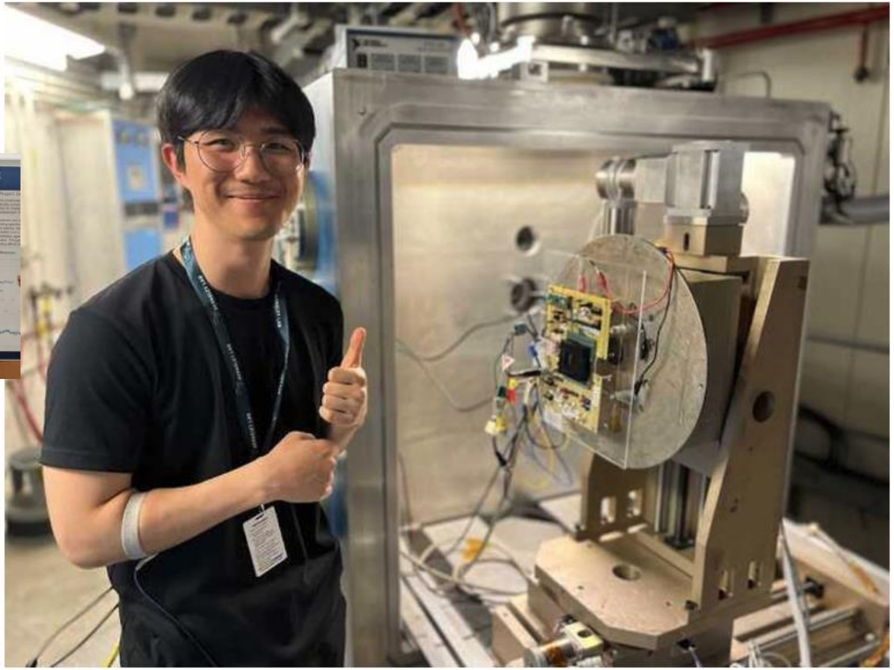
- The customer required assessment of radiation vulnerabilities
- The DIB needs workforce
- The problem …
  - Strategic Radiation Hardened Electronics Council (SRHEC) Single Event Effects (SEE) Testing Analysis of Alternatives (AoA) identified in FY21 a 5,000 hour per year shortage of SEE beam-time
  - Since that study, US nuclear modernization is further increasing test demand at heavy ion facilities – these facilities also support increasing commercial consumption



- **Limited number of heavy ion test facilities, with limited capacity, and highly competitive user base**
  - **Growing demand for time requires improved test efficiency of this resource**

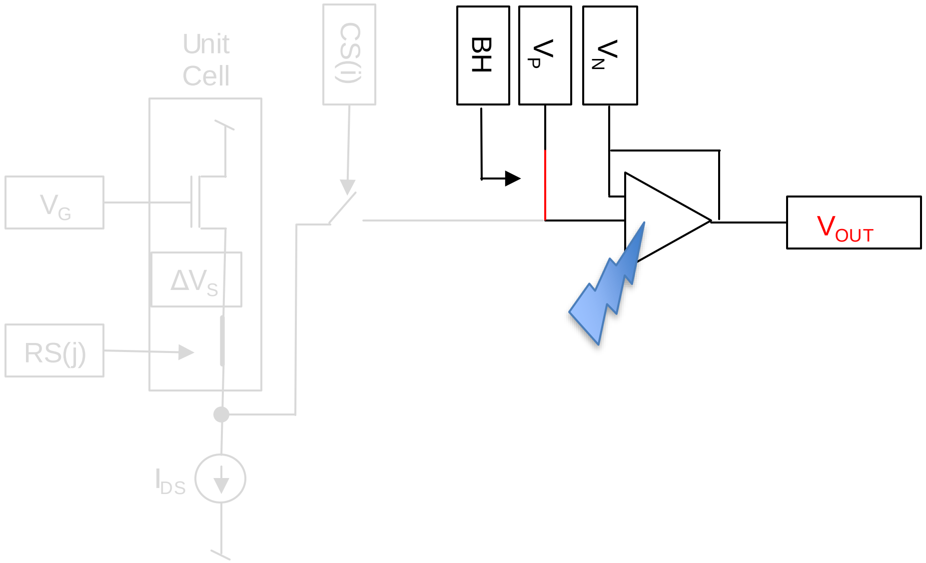
Source: Ahlbin, MDA

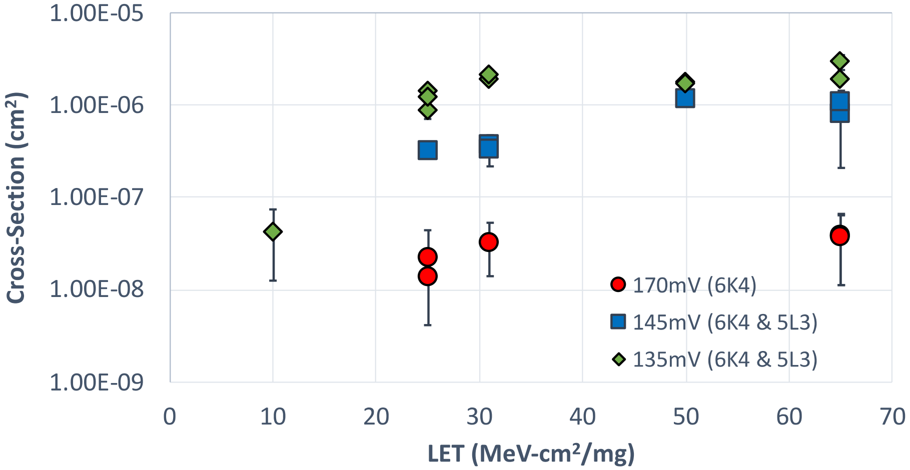
On-Site Workforce Training



IU graduate student Jaekon (Jay) Kim stands in front of his experiment at the Lawrence Berkeley National Laboratories 88" Cyclotron Facility in September 2023. IU announced Oct. 10, 2023, it will invest $111 million over the next several years in the microelectronics industry. *Photo by Courtesy Photo / The Indiana*

Demonstration of Radiation Tolerance





FY23 Metrics

Funded Collaborations:

- Reliable Microsystems, LLC (L. Massengill and J. Kauppila)
- NSWC Crane (M. Gadlage and K. Perry)
- Vanderbilt University, Basic research in radiation effects mechanisms (M. Alles)
- Vanderbilt University, POLSIR Spacecraft (R. Bennartz)
- Purdue University, SCALE WFD (P. Bermel)
- Arizona State University, Radiation, RTN and cryogenic measurement (H. Barnaby)
- CFD Research Corporation, TRL maturation (of DTRA-IIRM findings) through DTRA SBIR Phase I and MDA STTR Phase II (K. Linga)
- Johns Hopkins Applied Physics Laboratory, Van Allen Probes and System Fault Modeling (J. Likar)
- NASA GSFC, Data and Subject Matter Expertise on NASA SpaceCube and System Modeling (M. Campola)
- University of Cadiz/European Space Agency, CubeSat Reliability Modeling (I. Mateos)

Category	#
Invention Disclosures	2
Research/Faculty Awards	1
Site Visits	2
Invited Talks	3
Conference Proceedings	4
Conference Presentations	6
Collaborations	11
Journal Publications	4
Graduate Researchers	7
Undergraduate Researchers	10
Capstone Students	10
Internships	7 +*18*
WFD Impact	35

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