Trusted Semiconductor Solutions Overview

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Why are we here today?

- TSS Capability Overview
- TSS Growth Focused on 3D System Design and Expansion into Indiana
- TSS Engineering Workforce Development

Development and Delivery of Trusted High-Reliability Microelectronics

- Digital, analog, and mixed signal integrated circuit design from concept to GDSII (foundry hand-off)
- Wafer fabrication at Trusted foundries, ITAR foundries, and approved off-shore foundries
- Wafer processing including probe, bumping, thinning, dicing, and wafer sort
- Custom package assemblies for system miniaturization (SiP) and extreme environments
- MIL-STD testing, assembly and qualification with production management and inventory control
- Expertise in radiation effects modeling, hardening by design, and comprehensive radiation testing

military/defense

space

avionics

industrial

TRUSTED Semiconductor Solutions™

Trusted Semiconductor Solutions Corporate Overview

- Small business concern
- Non-traditional Defense Contractor
- ITAR and EAR compliant
- DoD Category 1A Trusted Accreditation
  - Design, aggregation, and broker services
- AS9100 certified quality system
- Cybersecurity: NIST 800-171 compliant and pursuing CMMC level 3 certification
- Staff of 50+ engineers and growing
  - Average experience is 25 years at companies like Honeywell, LSI Logic, Cadence, Medtronic, TI, Broadcom, Rockwell Collins, NASA, Intel, AMD
- Founded in 2006
- Located in Brooklyn Park, MN USA

NIST
800-171
Compliant

TRUSTED
Semiconductor Solutions™

TSS Vision Statement

To be the recognized leader in the implementation of high reliability microelectronics that are designed and built in the U.S.A

TSS Mission Statement

… to provide a complete solution for our customers “Trusted” semiconductor needs using on-shore resources while meeting the most stringent requirements of government, military, intelligence, aerospace, and industrial markets.

TSS Values

Technical excellence

Results oriented thinking

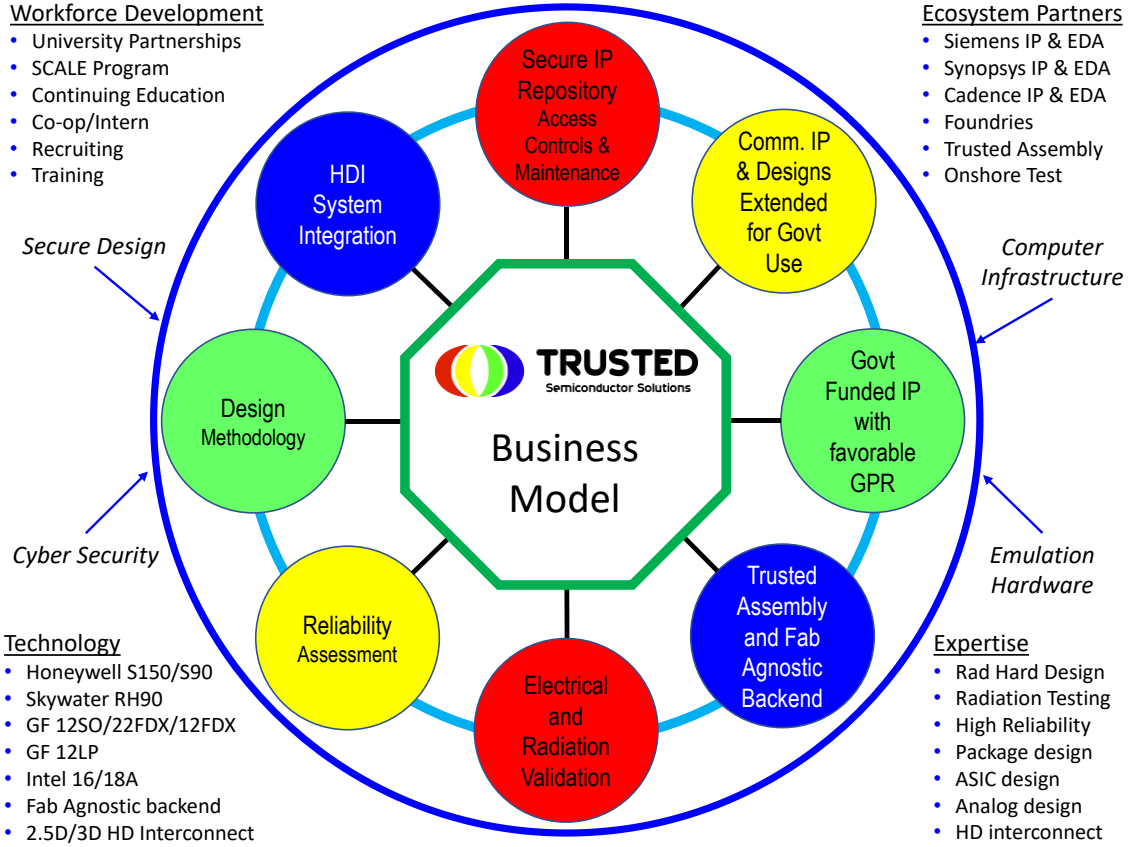
Unsurpassed program execution

Superior customer focus

Take ownership

TSS Business Model

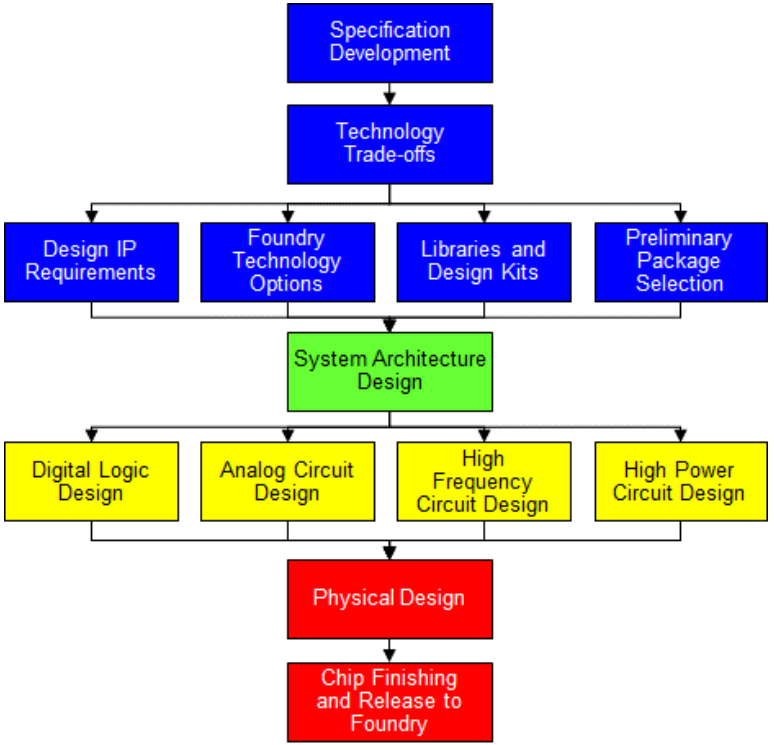
- Headquartered in Minnesota
- Expansion into Indiana
- Replicate the company culture



Technical Capabilities

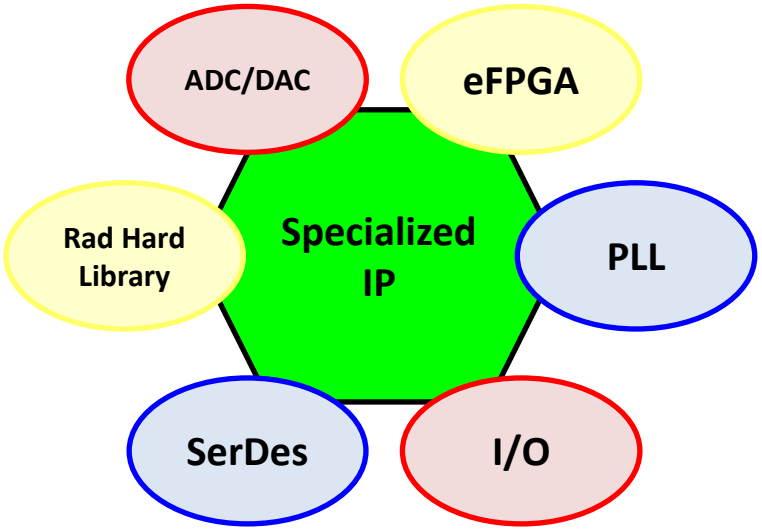
Trusted Semiconductor Solutions IC Design Capabilities

- Collaborative design environment where TSS engages with the customer in any (or all) of the following:
  - IC Specification Development
  - Implementation Trade-offs
    - Evaluation of IP options
    - Foundry selection
    - Package and assembly plan
    - Design for Test Methodology
  - Architecture Trade and Design
  - Front-end ASIC Design
  - Back-end ASIC Design
  - Final GDSII Release to Foundry
- Expertise in radiation hardened microelectronics

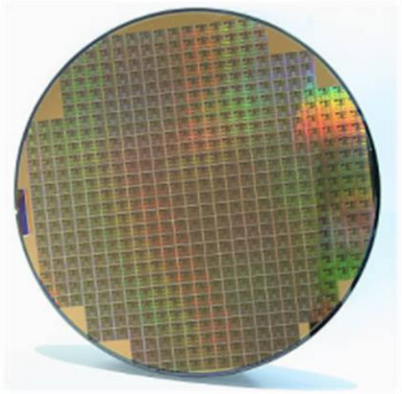


Specialized IP Development

- Trusted Semiconductor Solutions develops IP to enable ASIC and SoC designs
  - IP can be reused and relicensed for alternative applications/customers
  - IP portfolio driven by customer needs/requirements
- Expertise in radiation hardened IP
  - SerDes, eFPGA, I/O, memories, PLL, rad hard library, data converters
  - IP developed at 350nm, 180nm, 90nm, 45nm, and 12nm for a variety of foundries



Foundry Partnerships Enable Advanced, Radiation Hardened, and Legacy ICs



- Technology available for a wide variety of applications
  - CMOS, SOI, SiGe, BiCMOS
  - 1μm down to 7nm
  - Trusted, ITAR, on-shore and off-shore options
  - Radiation hardened libraries, IP, and design kits
- Trusted Semiconductor Solutions hands off design database, monitors manufacturing, and receives wafers

Tower Semiconductor
X-FAB MIXED-SIGNAL FOUNDRY EXPERTS
NXP
ON Semiconductor
SkyWater
intel
GLOBAL FOUNDRIES
Honeywell
tsmc

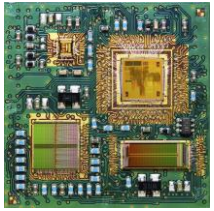
Secure eASIC Design Center

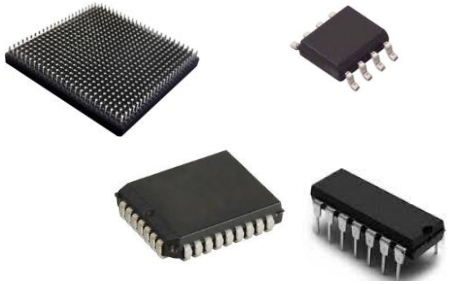
- TSS named as Intel eASIC Design Center in 2021
  - NIST compliant information system with DoD cybersecurity controls
  - Cleared, possessing facility with approved IS for classified IC design
  - Located in Minneapolis, Minnesota
- TSS team trained on the eASIC design methodology (FPGA to structured ASIC) and physical design
  - All eASIC tools installed and team is ready to execute designs
  - Intel 22FFL libraries installed
- All engineers are US citizens (40 engineers)
  - Trusted Accreditation enables TSS to clear as many engineers as needed
- Vast Experience porting FPGAs to ASICs (all FPGA vendors)
- Strong DIB and DoD relationships
  - Already engaged with all Tier 1 Defense Industrial Base (DIB) and the USG

Traditional Packaging for High Reliability Applications

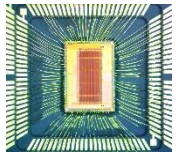
- Custom package design
  - Substrate, lid, and heat sink design
  - Analysis of die to package interface
    - Signal integrity, thermal, and power analysis

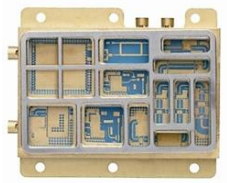
- Wide variety of advanced and legacy package configurations
  - Hermetic ceramic (CQFP, CBGA, CCGA, etc.)
  - Legacy (PLCC, DIP, SOIC, SOIC, etc.)
  - Advanced (WSP, CSP, ultra-fine pitch BGA, etc.)
  - 2.5D/3D
  - High power (metal, T0-style, cans, etc.)
  - System-in-Package (SiP) and Multi-Chip Modules (MCM)





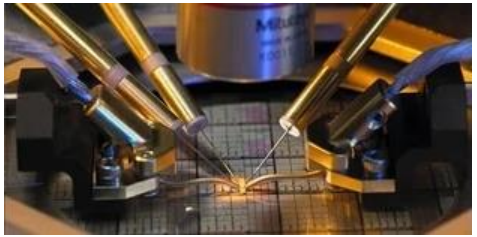
- Assembly of die into packages
  - Wirebonding, flipchip, die stacking, etc.
  - Molding, lid attach, glob top, etc.
  - Part marking

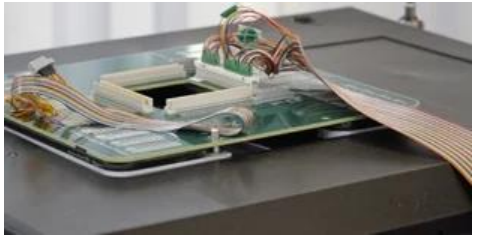




Characterization, Test, Screening, and Qualification

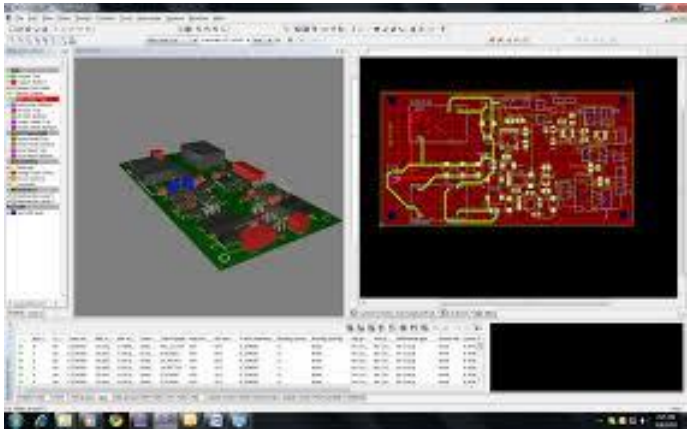
- Wafer Probe
  - Static testing including IDDQ
  - Dynamic testing depending on ASIC functionality
- Package Level Test
  - Static and dynamic testing
  - Electrical and functional test over temperature (-55C to 125C for military)
- Test Software and Hardware Development
  - Tester, handler, and test socket selection
  - Load board design and fabrication
  - Probe card design and fabrication
  - Printed circuit boards for characterization and test
- MIL-PRF-38534/5 or ESCC900 Screening and Qualification
  - HTOL, HAST, Temperature Cycling, Pre-conditioning, MSL rating, ESD, etc.
  - Bond pull, Die Shear, Shock, Seal Test, SEM, X-ray, Solderability, etc.
  - Burn-in and Life Test
- Device Characterization
  - Bench testing to validate and characterize a new ASIC design





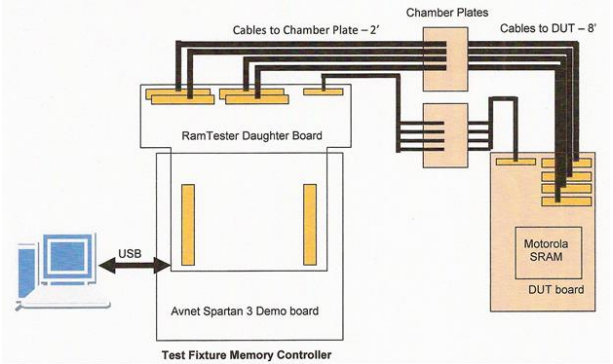
Printed Circuit Board Design Expertise

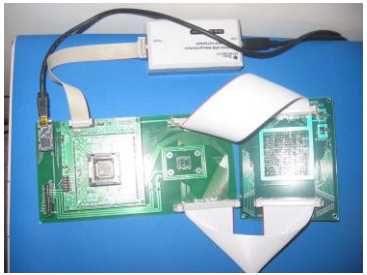
- Board Design
  - Single and double-sided boards
  - Multi-layer boards with buried/blind vias
  - Ultra-high speed, differential pairs, controlled impedance
  - Signal integrity and power analysis
  - BOM creation and management
  - Zuken, Altium, Eagle, Mentor PADS, and Cadence design tools
- PCB Substrate Technology
  - FR4, BT, LCP, and other custom substrates
  - Rigid and flex boards
- Design Services
  - Turn-key board design to assembly delivery
  - Augmentation services
  - Test and characterization capabilities



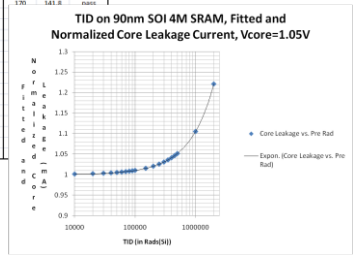
Comprehensive Radiation Test and Characterization of Integrated Circuits

- Study performance and existing radiation data on integrated circuit
  - Focuses radiation test plan to key areas of concern
- Develop radiation test and characterization plan
- Design and build radiation test hardware and software
  - Custom PCB boards for TID, SEE, and Dose Rate testing
  - Test software exercises parts and captures test data
- Prepare DUT samples for accurate SEE radiation testing
  - Package backside thinning
  - Die thinning
  - Custom sockets
  - Die extraction and repackaging
- Perform radiation testing
- Analyze test data and report findings
- Recommend radiation hardening approaches





TID	Voltage			DUT Measured Parameters					
				Dynamic Pattern			Complement Dynamic Pattern		
(rads(Si))	Core (volts)	IO (volts)		Core (mamps)	IO (mamps)	Functional pass/fail	Core (mamps)	IO (mamps)	Functional pass/fail
pre-rad	1.05	2.75		167	153.6	pass	167	152.8	pass
10K	1.05	2.75		167	146.9	pass	168	146.9	pass
20K	1.05	2.75		168	143.5	pass	169	144.3	pass
30K	1.05	2.75		168	142.7	pass	169	142.7	pass
40K	1.05	2.75		169	141.8	pass	170	141.8	pass
50K	1.05	2.75		170	141	pass			
60K	1.05	2.75		170	140.1	pass			
70K	1.05	2.75		170	140.1	pass			
80K	1.05	2.75		170	140.1	pass			
90K	1.05	2.75		170	139.3	pass			
100K	1.05	2.75		170	140.1	pass			
150K	1.05	2.75		171	141.8	pass			
200K	1.05	2.75		172	151.9	pass			
250K	1.05	2.75		172	170.5	pass			
300K	1.05	2.75		174	199.2	pass			
350K	1.05	2.75		175	227.9	pass			
400K	1.05	2.75		176	254.1	pass			
450K	1.05	2.75		177	277.7	pass			
500K	1.05	2.75		178	289.5	pass			



Expertise in Radiation Effects includes RHBD, Modeling and Radiation Testing of Electronics

Analysis

Monte Carlo particle simulations of neutrons, photons, heavy ion, and electrons impact on semiconductor materials

Modeling

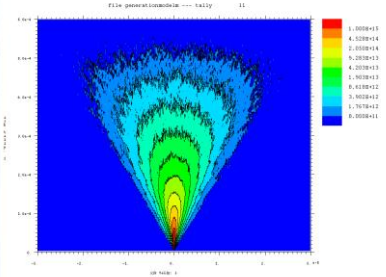
3D TCAD simulation of the semiconductor device structure with the added impact of radiation deposition

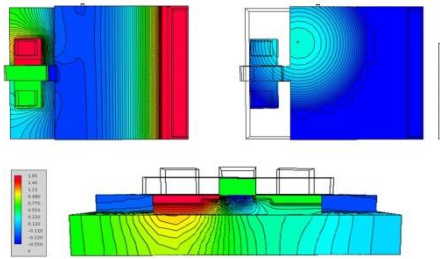
Design

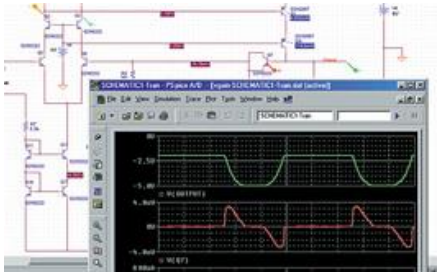
Rad-hard-by-design techniques are used during circuit design and layout to mitigate radiation effects

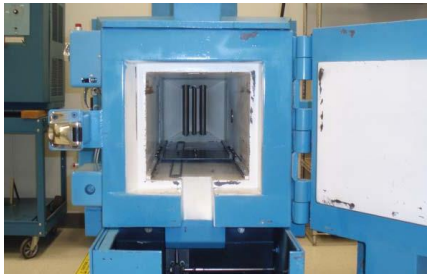
Validation

Device characterization includes total dose, dose rate, single event effects, neutron, and latch-up radiation testing





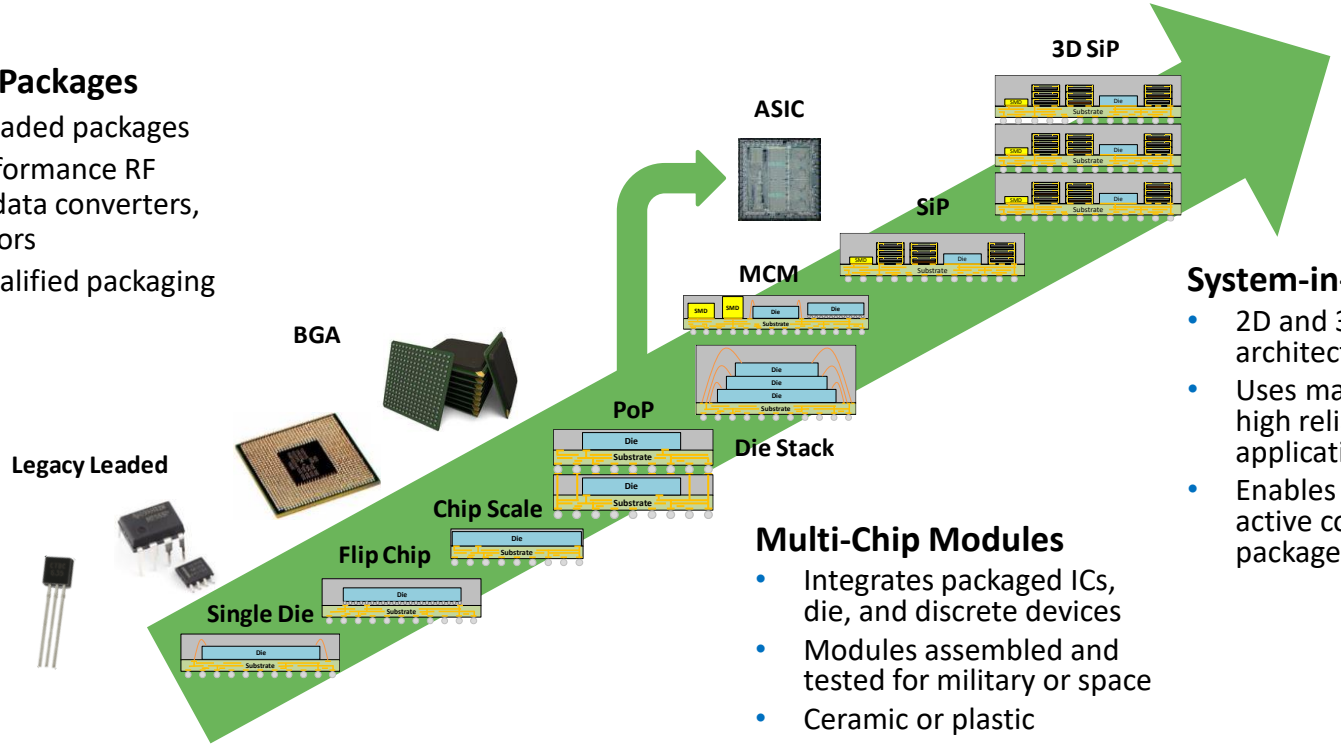




Advancing High Reliability Packaging to Enable Next Generation Military and Space Applications

Custom IC Packages

- Legacy leaded packages
- High performance RF circuits, data converters, and sensors
- Space qualified packaging



Multi-Chip Modules

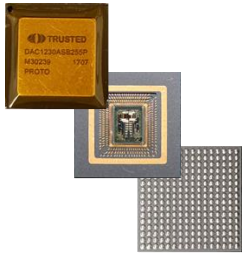
- Integrates packaged ICs, die, and discrete devices
- Modules assembled and tested for military or space
- Ceramic or plastic

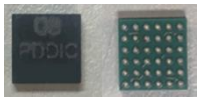
System-in-Package (SiP)

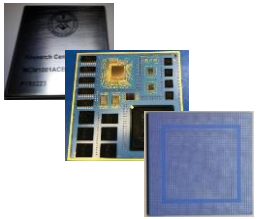
- 2D and 3D scalable architectures
- Uses materials suitable for high reliability and space applications
- Enables integration of active components in package substrate

Partnerships Enable Design, Manufacture, and Assembly of IC Packages in the USA

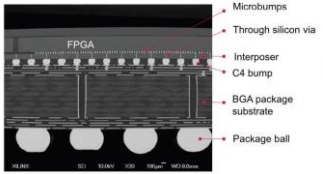
- Space-grade packages
  - High (HTCC) and low-temperature co-fired ceramic substrates (LTCC)
  - MIL-STD assembly and testing to Class V (space grade)
- Plastic packages
  - BGA, QFN, PLCC, flat pack, WSP, etc.
  - JEDEC standard configurations
- Multi-chip Modules (MCM)
  - Integrates die, packaged parts, and passives into a miniaturized system
- High-power packages
  - Metal cans, TO-style, etc.



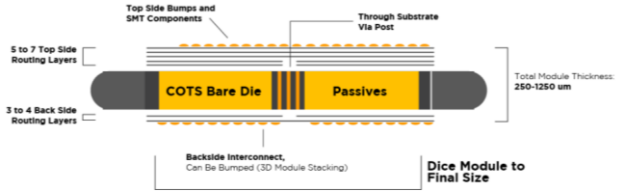




- Silicon interposers
  - Actively engaging with customers on high-density assemblies using Si interposer technology
  - Performing substrate design with signal integrity, thermal, and power analysis of system



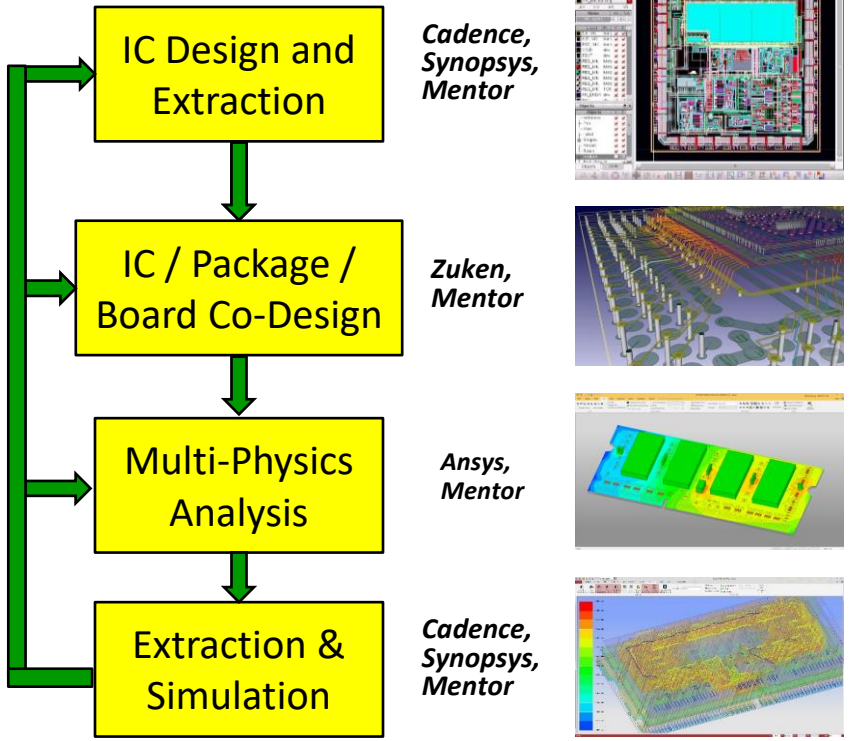
- Heterogeneous System in a Package (HSiP) technology (i3 Microelectronics)



TRUSTED Semiconductor Solutions™

Concurrent Development Flow Enables Design and Analysis of Integrated IC, Package, and PCB System

- Substrate selection to meet reliability and performance
  - Ceramic (HTCC and LTCC)
  - Plastic (BT and LCP)
  - Metal for high power
- Substrate and interposer design
  - Floorplanning, redistribution, and routing
- Co-design between IC design, system implementation, and performance analysis
  - Signal integrity
  - Power analysis
  - Thermal analysis
- Bonding diagrams
- Lid design



Track Record of Delivering Solutions

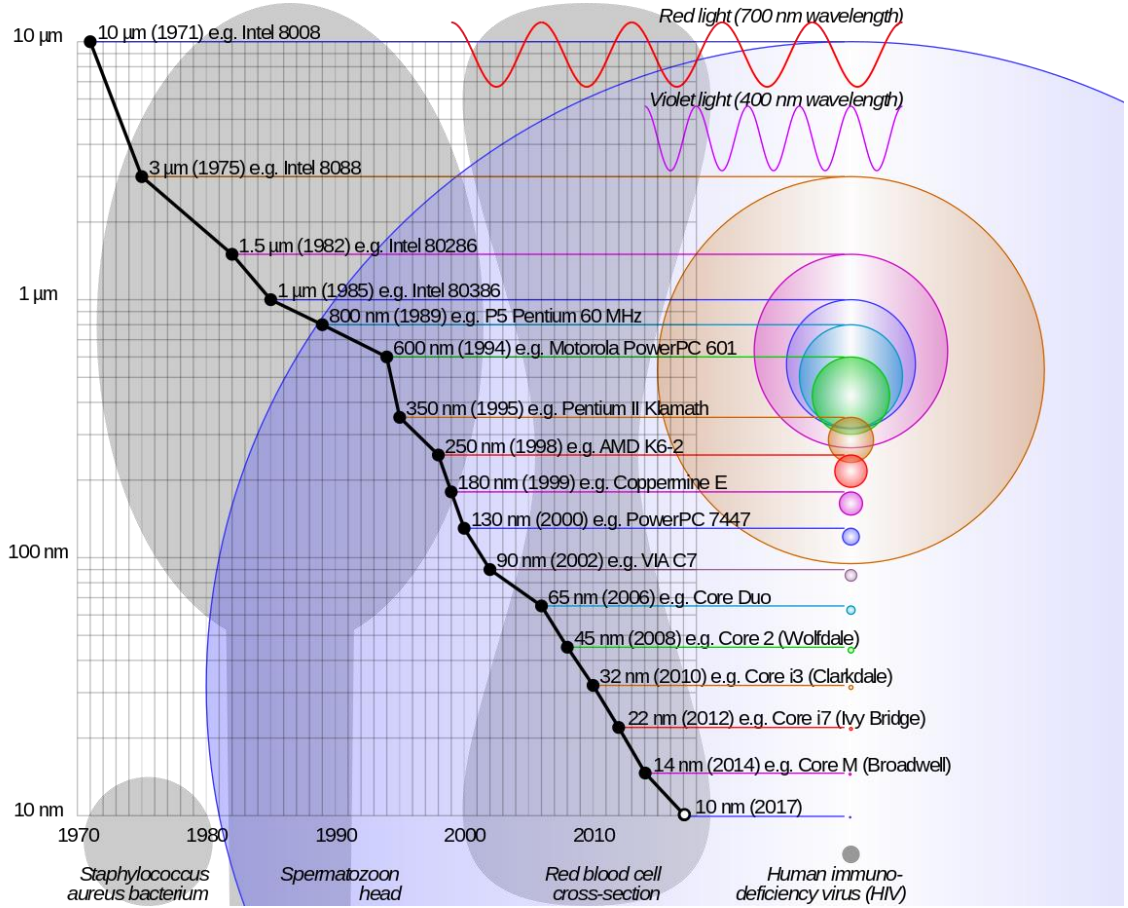
Proven Relationships, Contract Performance, and Product Deliveries to Mil-Aero, Industrial, and Commercial Markets

Delivering High Reliability Semiconductors to the Mil-Aero Marketplace for over 16 Years

TSS Focus Areas for Continued Growth

- Expand ecosystem partnerships with foundries
  - Intel
    - Productize ASIC flow and toolkit to support ASIC/SoCs
    - Grow IP portfolio on Intel16
    - Initial Intel 18A product development
  - GlobalFoundries
    - Grow IP portfolio on 45nm, 22nm, and 12nm processes
  - SkyWater
    - QML qualification of RH90 technology
    - Expand IP portfolio on RH90 technology
  - Expand relationships with XFab, ON Semiconductor, Tower Semiconductor, and Honeywell SSEC
- Enhance TSS in-house test and characterization capabilities
  - Wafer probe, package level testing, and device characterization testing
- Grow our 3D system and package design capabilities to support the 3D package manufacturers
- Grow portfolio of IP, chiplets, and standard products
  - IP Products
    - SOTP (90nm and 45nm)
      - Expand IP portfolio on GF 12SO and SkyWater RH90
      - Port IP developed on RH90 to GF 12SO
    - SOTA (22nm and below)
      - Develop IP portfolio to support high-reliability and rad hard applications
    - IP roadmap: UCIe, AIB, PCI-e, ADC/DAC, USB, Ethernet, DRAM3/4, MRAM, RISC-V, Cyber Security IP
  - Chiplet Products
    - Develop chiplets of key IP and productize
    - Chiplet roadmap: interface adapter (UCIe, DDR, JESD204), memories, FPGA, Cyber Security, Radiation Circumvention
  - Standard Products
    - Rad hard memories, processors, FPGAs, data convertors
    - Nuclear event detectors and circumvented COTS devices
    - Products that operate in extreme environments
    - Legacy part replacements

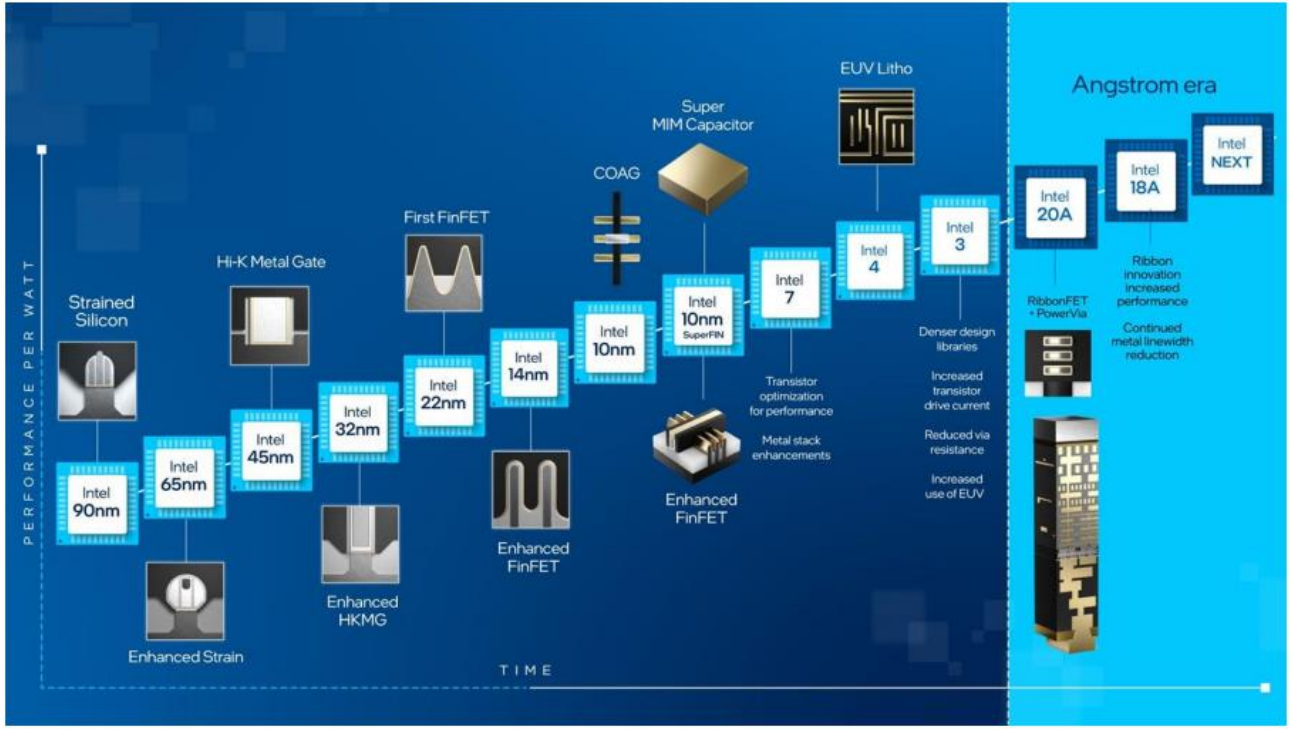
TSS Growth Focused on 3D System Design and Expansion into Indiana



Transistor Scaling Approaches Limits

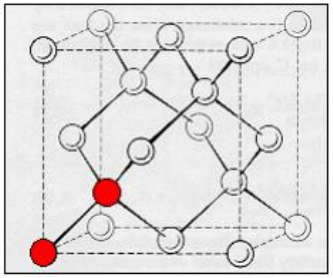
- Started developing IC's at 1500nm geometry
- In 2024, TSS will be designing products with 1.8nm technology
- Nearing the physical limit of monolithic SoC solutions

IC Technology Scaling Approaching Atomic Scale



Source: Intel

Silicon



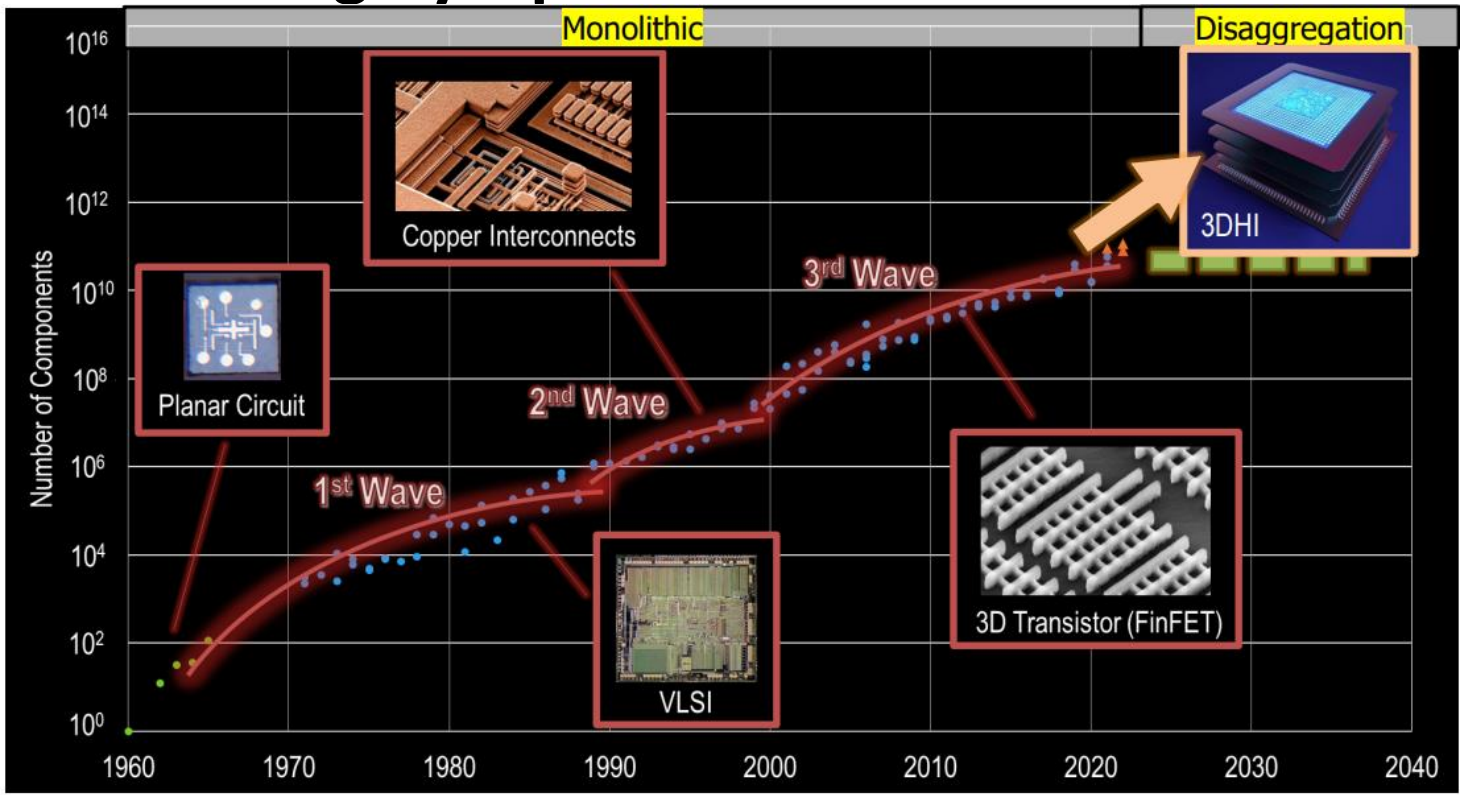
Source: Princeton

Nearest neighbor: 0.235 nm
Lattice parameter: 0.543 nm

Other scaling failure modes

- Leakage current increase
- Transistor turn-off / turn-on
- Oxide layers
- Barrier layers
- Contact quality
- Transistor area

Path Forward: 3D Systems that are comprised of Highly Optimized IC Functions



TSS Growth Will Be Driven by Designing Highly Optimized 3D Systems using Onshore Resources

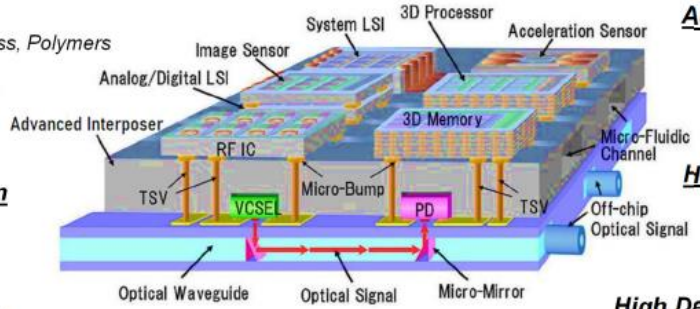
3-D Packaging CAD Tools
Si, SiGe, GaN, GaAs, InP, Glass, Polymers
RDL
3-D Stacking
FO-WLP

Wafer Preparation
Si, SiGe, GaN, GaAs, InP, Glass, Polymers
RDL
Wafer Thinning
Temp Wafer Bonding/De-Bonding
Die Attach Film (DAF)
Die Singulation

Wafer-Level High Density Interconnects
Si, SiGe, GaN, GaAs, InP, Glass, Polymers

Advanced Thermal Technologies
Si, SiGe, GaN, GaAs, InP, Glass, Polymers
1000 – 2000 W/m°K
Integrated Solutions
Active/Passive Cooling

Wafer Bumping
Si, SiGe, GaN, GaAs, InP, Glass, Polymers
Pad Finish
Under Bump Metallurgy (UBM)
C4 Bumping
Cu Pillar Bumping



Advanced Test and Failure Analysis
High Speed Digital
High Frequency RF
Test 3-D Architectures

Si Interposer Fabrication
RDL Top and Bottom
TSV
Embedded Passives
Wafer Bonding
RF Friendly Film Deposition
Interposer Test
III/V Interposer Fabrication

High Density Interconnect (HDI) PCBs
Up to 36 Layer Boards
High Density Lines/Spaces
IPC-2226 Standard for HDI Design

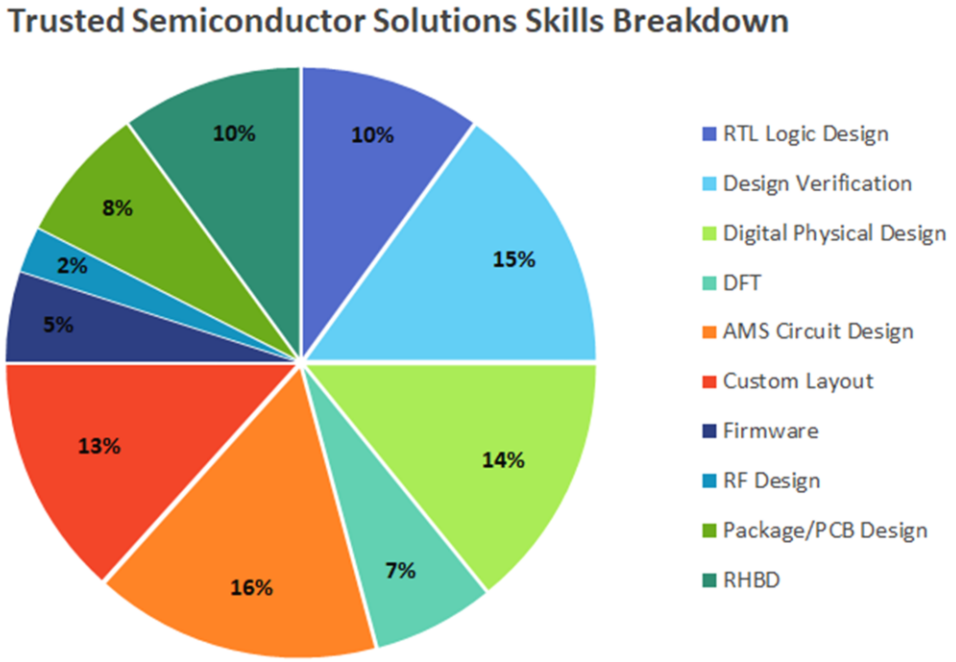
Fan-Out Wafer-Level Packaging (FO-WLP)
Reconstituted Wafer
Si, SiGe, GaN, GaAs, InP, Glass, Polymers
RDL
Integration of RF, mmWave, Digital Components

Classified Interposer Assembly
Classified Hardware and Test
3-D Assembly
Wafer-to-Wafer Bonding
Thermo-Compression Bonding (TCB)
Die-to-Wafer Stacking
Die –to-Die Stacking

High Density Build-Up (HDBU) Substrates
20+ Layers
9 Build Up Layers Each Side
Up to 4 Cores
High Density Lines/Spaces

BEOL Processing
300mm Wafer Processing
Panel Processing

Current TSS Engineering Skillset that will need to be Multiplied in Indiana and Minnesota



- Development team (ITAR compliant) has experience designing 100's of ICs for 1.5um down to 5nm
- TSS specialization in design of strategic radiation hardened microelectronics
- TSS expertise in IC and custom package design for high-reliability applications
- Long-standing relationships with Synopsys, Cadence, and Siemens (> 20 years)
- Ability to clear designers for classified programs
- Manufacturing partners for wafer fab, package substrates, die assembly, electrical, mechanical, and reliability testing
- Full-development flow from concept to qualified part delivery

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TSS Company Culture

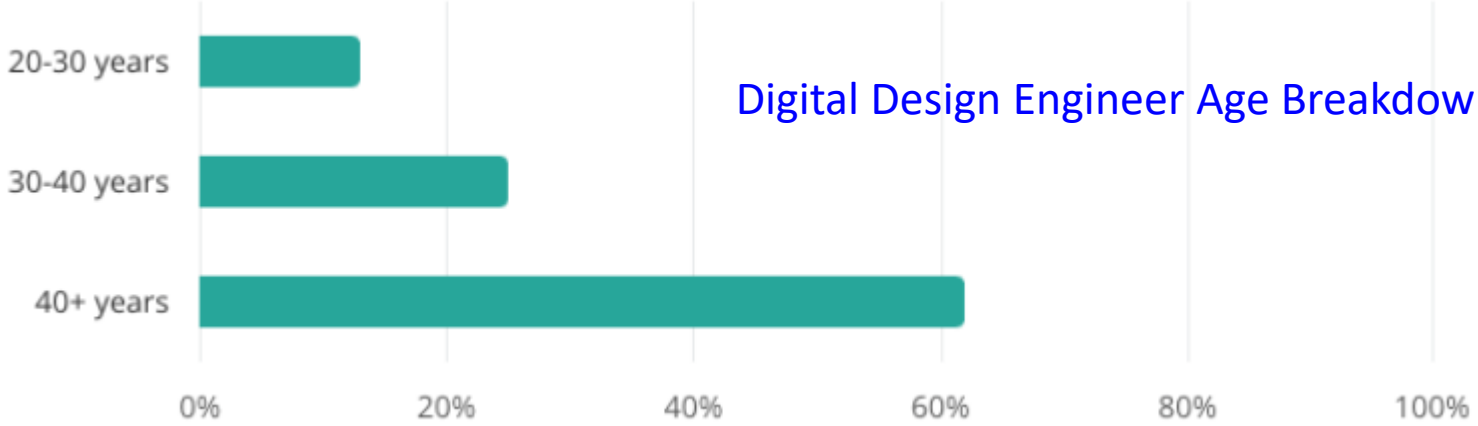
Kendall Diveley

Engineering Workforce Development

Outline

- Long-Term Focus
- Mentorship
- Performance Reviews
- Company Activities
- Work-Life Balance
- Constant Iteration

Current Obstacles Recognized and Being Actively Addressed at TSS

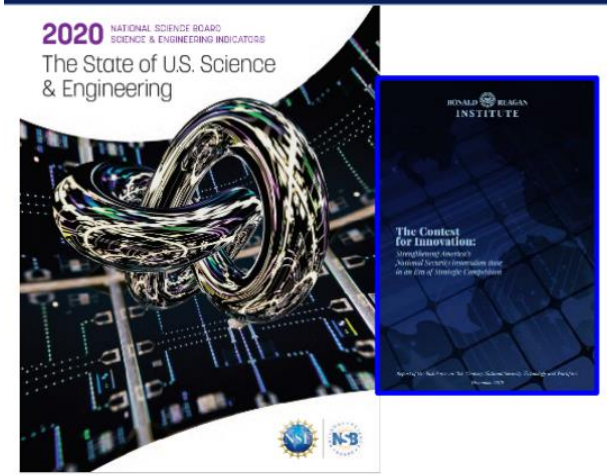


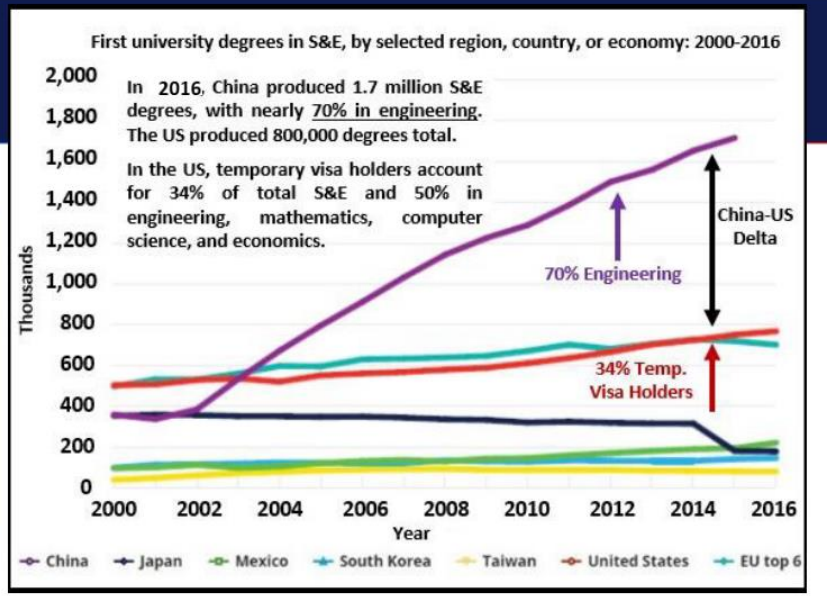
Digital Design Engineer Age Breakdown

- Current obstacles
  - Aging industry
  - Offshoring resulted in less US citizen candidates
  - Alignment of business culture to current generation motivation
    - i.e. the need to make a difference in society per Dr. Kerrie Douglas, Purdue University

Workforce Development is Critical to Reshoring Semiconductor Capability

STEM Talent Crisis





As much as emerging technologies will define future conflict, ***the war for talent will likely play the central role*** in the outcome of long-term technological competition.

The National Security Innovation Base (NSIB) struggles to attract, recruit, and retain a workforce willing and able to tackle tough challenges and find innovative solutions. Universities are confronting a dearth in American talent generation and retention. Much of that shortfall is filled with foreign students, a large share of them from China.

In 2018 TSS Focused on Addressing Flatten the Demographic Curve in Engineering

- Solutions:
  - Our focus is on hiring a mix of new and expert engineers as we grow
  - Utilizing our network of senior talent to train next generation on real programs with the Defense Industrial Base (DIB)
  - Develop relationships with local universities and students prior to graduation
    - Sponsor student projects
    - Mentor students
    - Offer internships
  - Most interns return as full-time employees
  - Constant re-evaluation of our approach

Mentorship

- Open-door policy / encourage questions
- Benefits both new and experienced engineers
- Teaches patience and communication skills
- Sets an example for the next generation

Performance Reviews

- Biannual reviews
  - Encourage professional and personal goals
  - Monitor progress on those goals
  - Help employees take ownership of their work
  - Encourage exploration of relevant technical areas of interest

Company Activities

- Helps to develop closer connections with coworkers
- Weekly all-hands lunch
- Periodic group outings
  - Collaboration
  - Competition
  - Variety of events

Work-Life Balance

- Personal freedoms encourage employees to work effectively
- Maintains positive feelings about the workplace
- Outside interests often positively impact the work environment

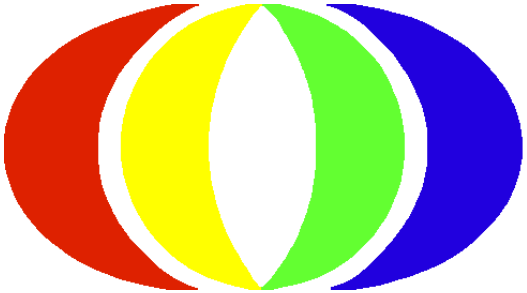
Constant Iteration

- At TSS, we approach company culture much like technical work
  - Research and Intuition
  - Action
  - Observation of results
  - Iteration
- Management is great at providing and accepting feedback
  - Lead by example
- Low attrition rate
  - Employee retention consistently at or above 95%

Growth in Indiana

- Alignment of curriculum to TSS needs
  - K-12, trade schools, and universities
- TSS wants sponsor student projects to develop real world products
  - FPGA, PCB, advanced packaging design, cybersecurity, etc.
- Internship and Coop opportunities locally
- Cross-pollination of people in MN and Indiana team to ensure similar company culture development
- Scale the business model in Indiana

Questions and Answers



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